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Design of Low Voltage and High Speed Double-Tail Dynamic Comparator for Low Power Applications

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Abstract: *Comparators are basic building elements for designing modern analog and mixed signal systems. Speed and resolution are two important factors which are required for high speed applications. This paper presents a design for an on chip high-speed dynamic latched comparator for high frequency signal digitization. The dynamic latched comparator consists of two cross coupled inverters comprising a total of 9 MOS transistors. The measured and simulation results show that the dynamic latched comparator design has higher speed, low power dissipation and occupying less active area compared to double tail latched and preamplifier based clocked comparators. A new fully dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators has been designed. With two additional inverters inserted between the input-stage and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented.*
Keywords: *Comparator, Double-Tail Comparator.*

I. Introduction

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to digital converters (ADCs), Memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee

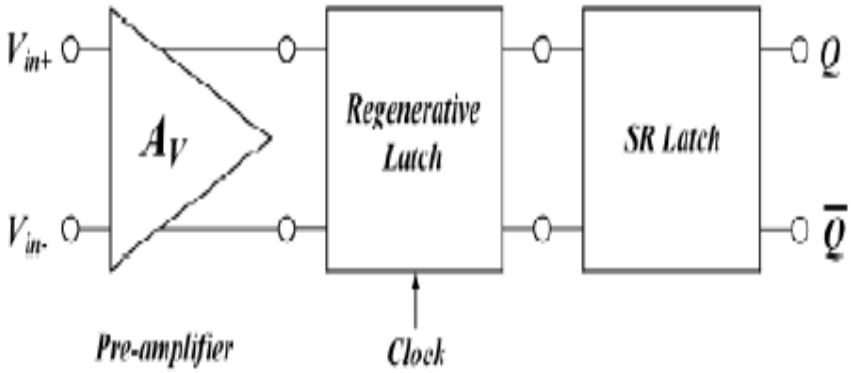


Fig 1 High speed voltage comparator

In this paper, we present a new dynamic latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 25% less input referred latch offset voltage and 44% less sensitivity of the delay versus the input voltage difference (delay/log(!Vin)), which is about 17.4ps/decade, than the conventional double-tail latched comparator at approximately the same area and power consumption.

II. Clockedregenerative Comparators

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Out*n* and Out*p* to *V*DD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8 are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where *V*INP > *V*INN, Out*p* discharges faster than Out*n*, hence when Out*p* (discharged by transistor *M*2 drain current), falls down to *V*DD–|*V*thp| before Out*n* (discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n* pulls to *V*DD and Out*p* discharges to ground. If *V*INP < *V*INN, the circuits works viceversa.

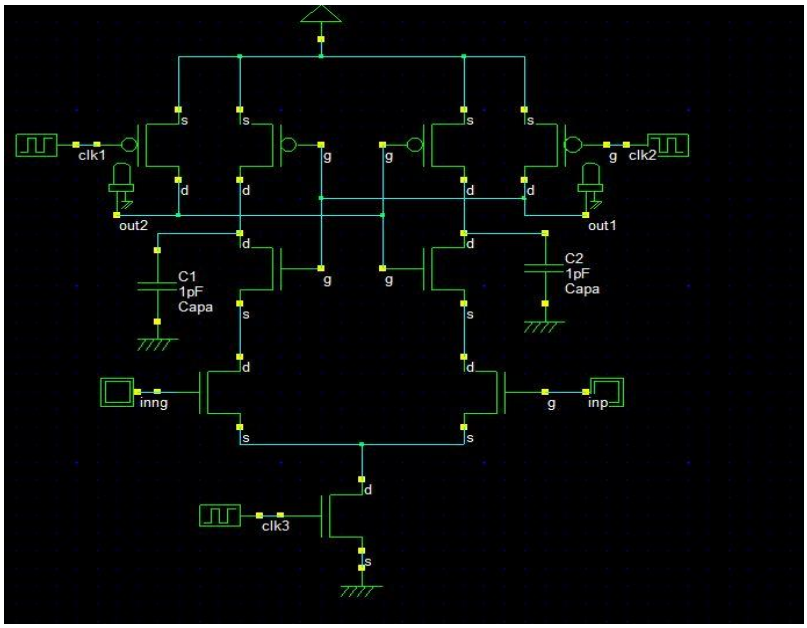


Fig2:Conventional Dynamic Comparator

As shown in Fig. 2, the delay of this comparator is comprised of two time delays, *t*0 and *t*latch. The delay *t*0 represents the capacitive discharge of the load capacitance *C*L until the first p-channel transistor (*M*5/*M*6) turns on. In case, the voltage at node INP is bigger than INN (i.e., *V*INP > *V*INN), the drain current of transistor *M*2 (*I*2) causes faster discharge of Out*p* node compared to the Out*n* node, which is driven by *M*1 with smaller current. Consequently, the discharge delay (*t*0) is given by

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \cong 2\frac{C_L |V_{thp}|}{I_{tail}}.$$

In (1), since *I*2 = *I*tail/2 + _*I*in = *I*tail/2 + *g*m1,2_*V*in, for small differential input (_*V*in), *I*2 can be approximated to be constant and equal to the half of the tail current. The second term, *t*latch, is the latching delay of two crosscoupled inverters. It is assumed that a voltage swing of _*V*out = *V*DD/2 has to be obtained from an initial output voltage difference _*V*0 at the falling output (e.g., Out*p*). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [17]. Hence, the latch delay time is given by, [18]

$$t_{\text{latch}} = \frac{C_L}{g_{m,\text{eff}}} \cdot \ln\left(\frac{\Delta V_{\text{out}}}{\Delta V_0}\right) = \frac{C_L}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (2)$$

where *gm,*eff is the effective transconductance of the back-toback inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at $t = t0$). Based on (1), _*V*0 can be calculated from (3)

$$\begin{aligned}\Delta V_0 &= \left|V_{\text{out}p}(t = t_0) - V_{\text{out}n}(t = t_0)\right| \\ &= \left|V_{\text{thp}}\right| - \frac{I_2 t_0}{C_L} = \left|V_{\text{thp}}\right|\left(1 - \frac{I_2}{I_1}\right).\end{aligned}$$

The current difference, _*I*in = |*I*1 − *I*2|, between the branches is much smaller than *I*1 and *I*2. Thus, *I*1 can be approximated by *I*tail/2 and (3) can be rewritten as

$$\begin{aligned}\Delta V_0 &= \left|V_{\text{thp}}\right| \frac{\Delta I_{\text{in}}}{I_1} \\ &\approx 2\left|V_{\text{thp}}\right| \frac{\Delta I_{\text{in}}}{I_{\text{tail}}} \\ &= 2\left|V_{\text{thp}}\right| \frac{\sqrt{\beta_{1,2} I_{\text{tail}}}}{I_{\text{tail}}} \Delta V_{\text{in}} \\ &= 2\left|V_{\text{thp}}\right| \sqrt{\frac{\beta_{1,2}}{I_{\text{tail}}}} \Delta V_{\text{in}}.\end{aligned}$$

In this equation, β1,2 is the input transistors' current factor and *I*tail is a function of input common-mode voltage (*V*cm) and *V*DD. Now, substituting _*V*0 in latch delay expression and considering *t*0, the expression for the delay of the conventional dynamic comparator is obtained as

$$\begin{aligned}t_{\text{delay}} &= t_0 + t_{\text{latch}} \\ &= 2\frac{C_L\left|V_{\text{thp}}\right|}{I_{\text{tail}}} + \frac{C_L}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{DD}}{4\left|V_{\text{thp}}\right| \Delta V_{\text{in}}} \sqrt{\frac{I_{\text{tail}}}{\beta_{1,2}}}\right). \quad (5)\end{aligned}$$

Equation (5) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance *C*L and inversely proportional to the input difference voltage (_*V*in). Besides, the delay depends indirectly to the input common-mode voltage (*V*cm). By reducing *V*cm, the delay *t*0 of the first sensing phase increases because lower *V*cm causes smaller bias current (*I*tail). On the other hand, (4) shows that a delayed discharge with smaller *I*tail results in an increased initial voltage difference (_*V*0), reducing *t*latch. Simulation results show that the effect of reducing the *V*cm on increasing of *t*0 and reducing of *t*latch will finally lead to an increase in the total delay. In [17], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

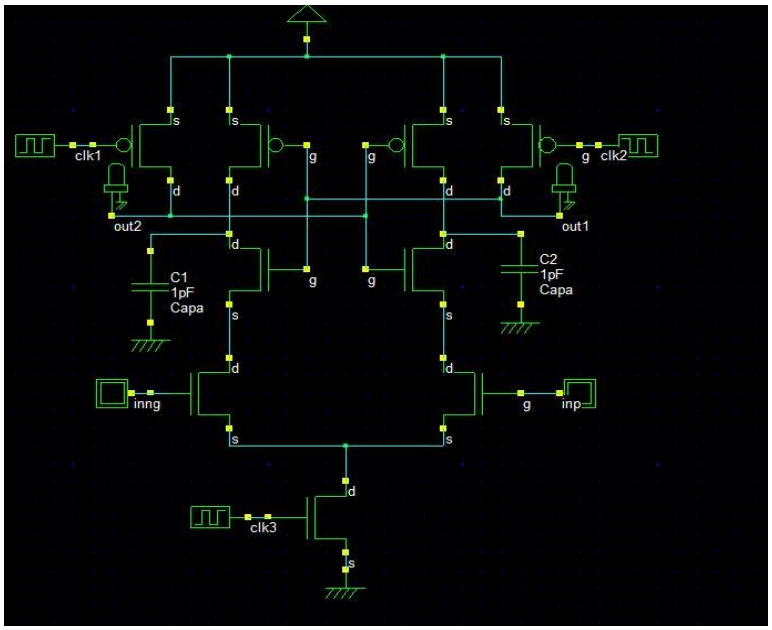


Fig 3: Schematic diagram of the conventional double-tail dynamic comparator.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low
Offset [10]. The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1*/C*fn(p*)* and on top of this, an input-dependent differential voltage _*V*fn(p*)* will build up. The intermediate stage formed by *M*R1 and *M*R2 passes _*V*fn(p*)* to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].
Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t* latch. The delay *t*0 represents the capacitive charging of the load capacitance *CL* out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9*/M*10) turns on, after which the latch regeneration starts; thus *t*0 is obtained.

III. Proposed Double-Tail Dynamic Comparator

Fig demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase _*V*fn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M3/M*4 transistors but in a cross-coupled manner[see fig4].

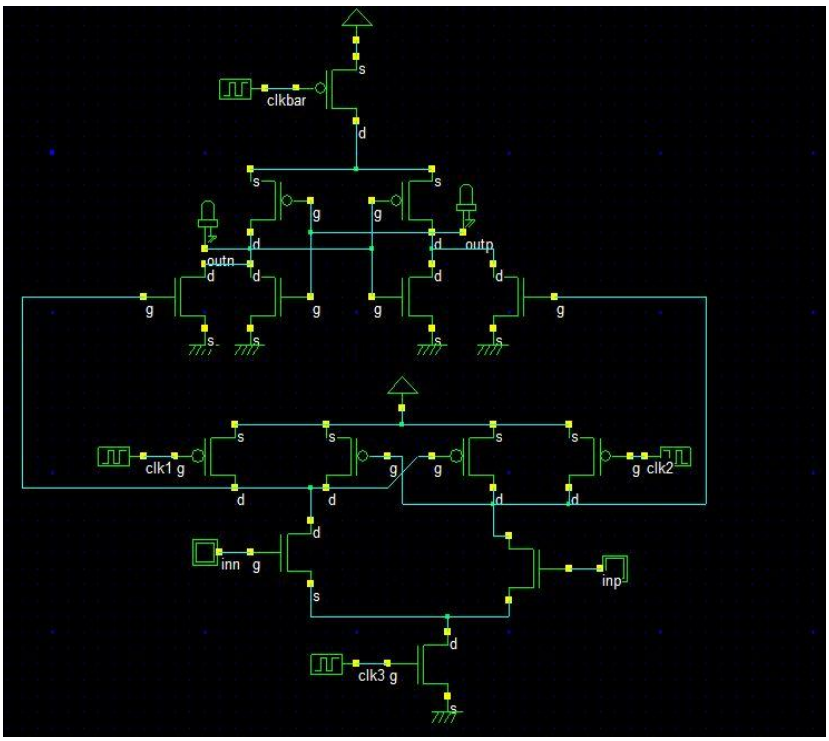


Fig4: Proposed Dynamic Comparator main idea.

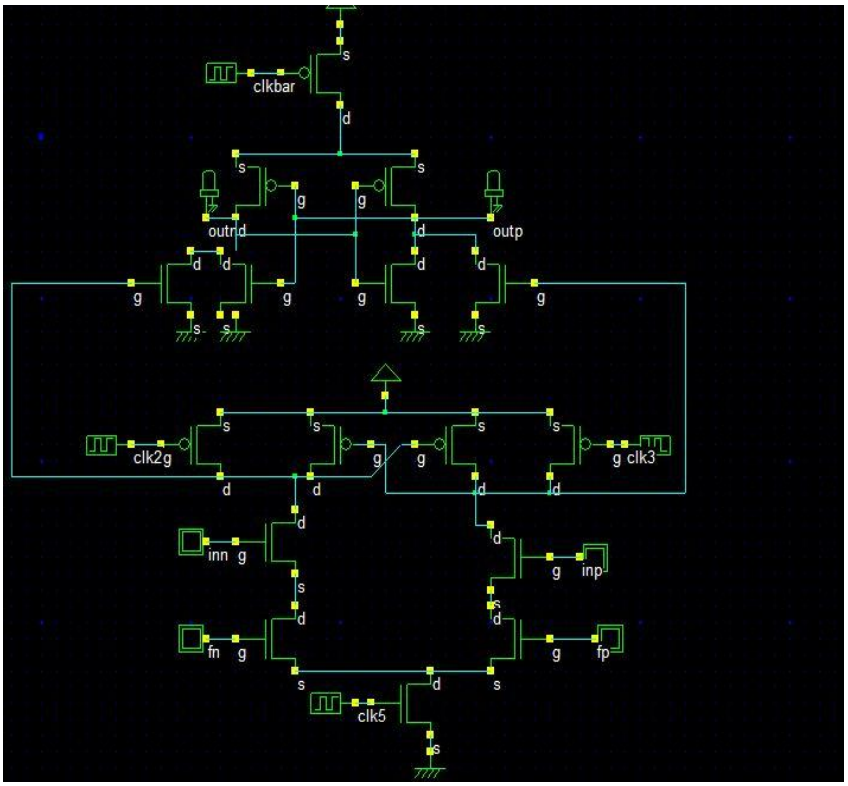


Fig5**: Final structure of the proposed double-tail comparator .**

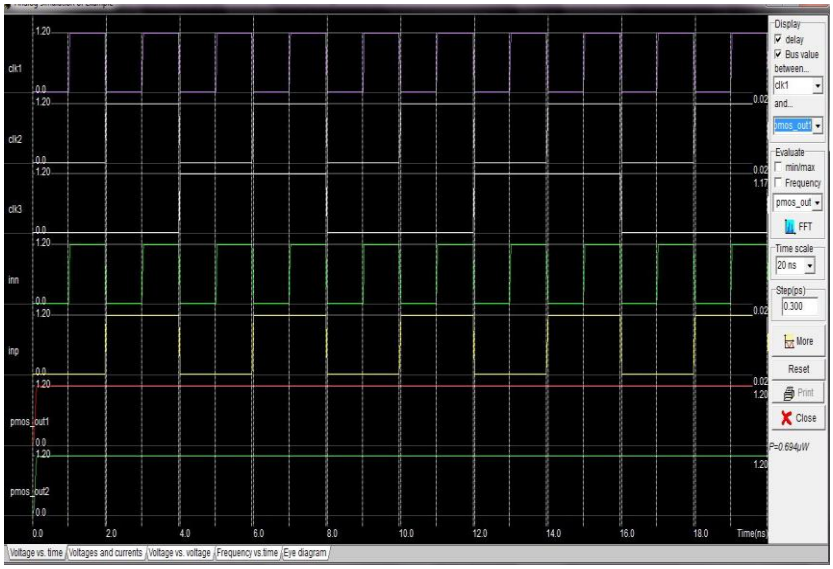
A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows (see Fig.. During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both Fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues falling, the corresponding PMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which _*V*fn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (*M*c1) turns on, pulling the other node fp back to the *V*DD. Therefore by the time passing, the difference between fn and fp (_*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B).

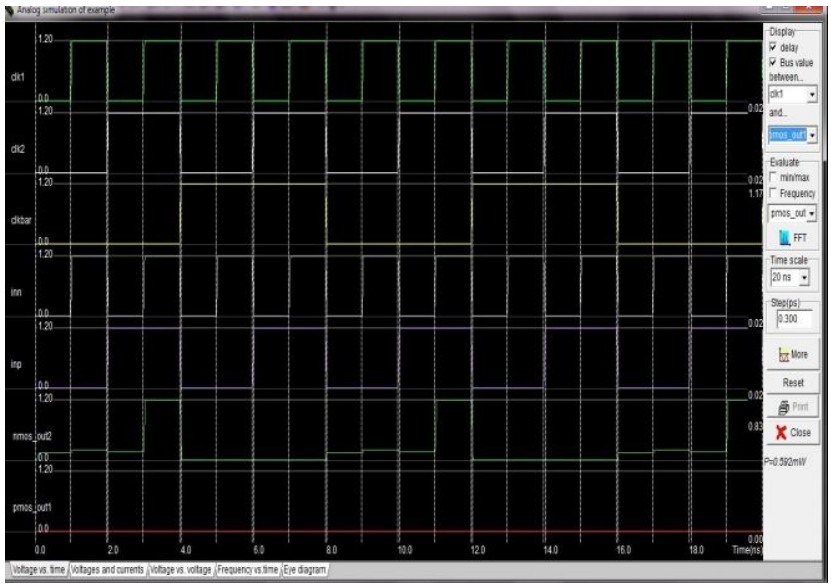
Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on, a current from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors [*M*sw1 and *M*sw2, as shown in Fig. 2(b)]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to *V*DD.

IV. Simulation Results

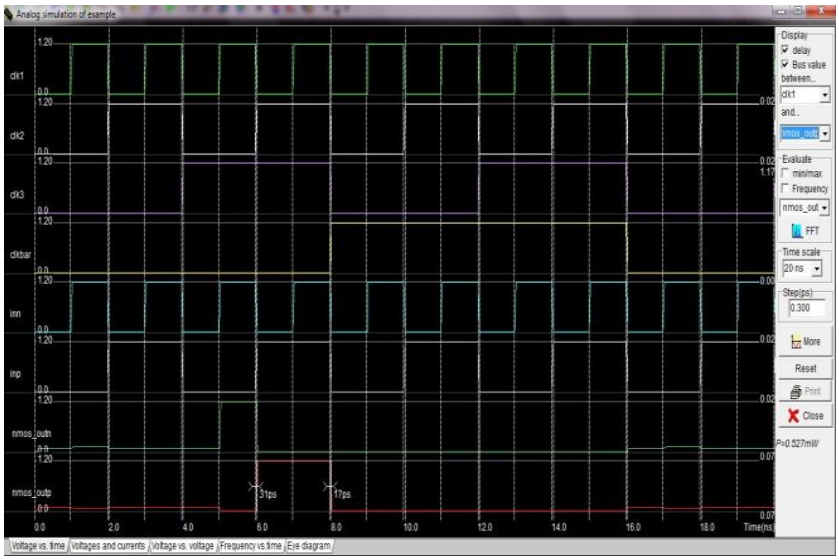
In order to compare the proposed double-tail comparator with the conventional double –tail dynamic comparators,all circuits have been simulated in 0.12-μm CMOS technology.



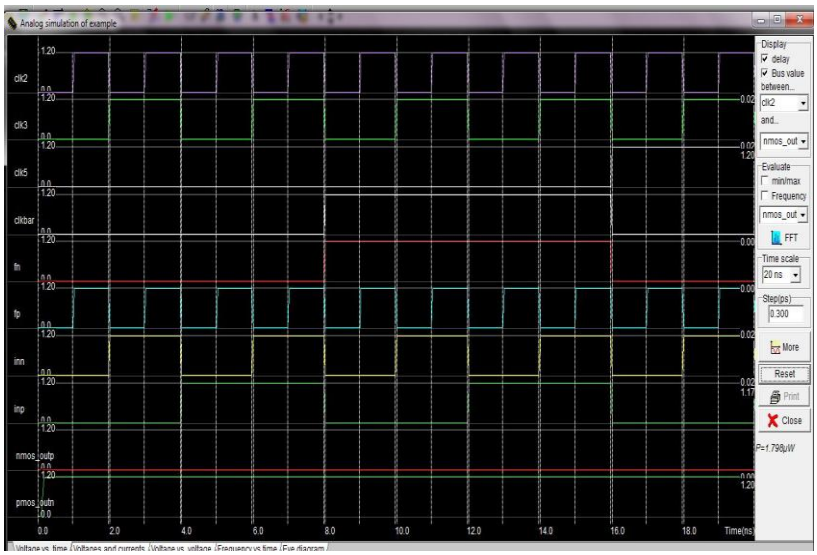
Timing Diagram of Conventional Dynamic comparator



Timing Diagram of Conventional double-tail comparator



Timing diagram of proposed dynamic comparator



Timing Diagram of proposed Dynamic Comparator

V. Conclusion:

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.12-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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