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Design of a low power 12bit SAR ADC with self calibration

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Abstract: *This paper introduces a low power 12bit SAR ADC for portable EEG sensor .The influence on accuracy capacitance error and parasitic capacitance is discussed in detail. An self-calibration circuit is designed on the traditional structure,it greatly reduces the effect of capacitance error and improve the conversion accuracy of ADC。The design adopts CMOS 0.13 □m process, the simulation results show that when the input signal bandwidth is 50Hz and the clock frequency is 7.8kHz with adding the calibration circuit， SNDR reached 71.47dB, and ENOR reached 11.51bit, and INL value decreased from 6LSB to 0.25LSB.The circuit adopts 1.2V power supply, power consumption is about 26□W, which can meet the requirements of application of portable sensors.*

Keywords: *EEG; SAR ADC; DAC; self-calibration*

I. INTRODUCTION

EEG (Electroencephalogram) monitoring is an important means for clinical diagnosis and disease prevention-control. In order to make a more comprehensive and accurate judgment of the human health, we need to monitor the EEG for a long time, and collect and analyze the information continuously. But the traditional EEG medical monitoring equipment can not continue for too much long time, so the research and application of EEG portable monitoring equipment gradually has become a hot topic.ADC (Analog to digital converter) is an important part of portable EEG sensors which can transform analog signals into the digital signals who can be applied to machine recognition. Portable sensors ADC need to work for a long time, therefore it is necessary to design the circuit with low power consumption. At the same time the circuit processing signal frequency is low, the high speed is not necessity. SAR ADC (Successive Approximation Register Analog-to-digital Conventer) has the characteristics of medium speed, medium precision and low power consumption which can meet the above requirements.Due to the current process conditions, SAR ADC is difficult to achieve requirements of the 12bit resolution, where the split capacitor charge redistribution DAC is affected by capacitor mismatch and parasitic capacitance. Therefore DAC circuit need to join the calibration technology to improve the resolution of ADC. Literature[1] adds adjustable capacitance to compensate the nonlinear error. But the chip area occupied by this structure is directly proportional to the precision after calibration, so it requires a great sacrifice of the chip area to achieve better accuracy, where is not suitable for portable devices. In literature [7], 11bit SAR ADC makes use of DAC self capacitance array self calibration by digital logic control instead of joining additional calibration circuits, which greatly reduce the chip area occupied. But by this method, the effective bits of calibration circuit can only reach 9.93bit, which is far lower than the resolution of the circuit requirements. In this paper, an adjustable capacitor circuit with the style of binary weighted capacitor array is connected between the low side capacitor array and the ground for calibration. Simulation results show that this design improves the ADC resolution and greatly reduces the chip area occupied by calibration circuit.

II. THE DESIGN OF SAR ADC

2.1 SAR ADC PRINCIPLE

As shown in Figure 1, SAR ADC is consisted of the sample and hold circuit, comparator, DAC and digital logic control circuit. Its working principle is based on the binary search algorithm: Firstly, DAC outputs a reference voltage; Then the reference voltage will be compared with maintained sampling input signal in the comparator; Thirdly, according to the output of the comparator, the digital logic control circuit is used to adjusts the output of DAC the voltage, which is aimed to let the output voltage of DAC gradually approach the input voltage; At last, repeat step three until the comparison is done with the last bit of the logic control circuit.

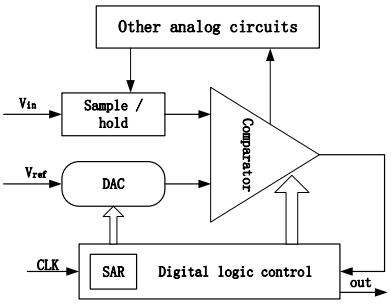


Fig.1 The structure of SAR ADC

2.2 DAC DESIGN WITH SELF CALIBRATION

According to the requirement of low power consumption of portable EEG sensor, in this paper, the DAC is designed by using binary segmented capacitor charge redistribution DAC structure. The structure of the the DAC circuit is mainly composed of capacitors, so this structure consumes less power than other ones[4]. As shown in Fig.2 (a), the traditional 12bit split capacitor charge redistribution DAC structure consists of a split capacitor C_s and a both-sides capacitor array. Its working principle is as follow:

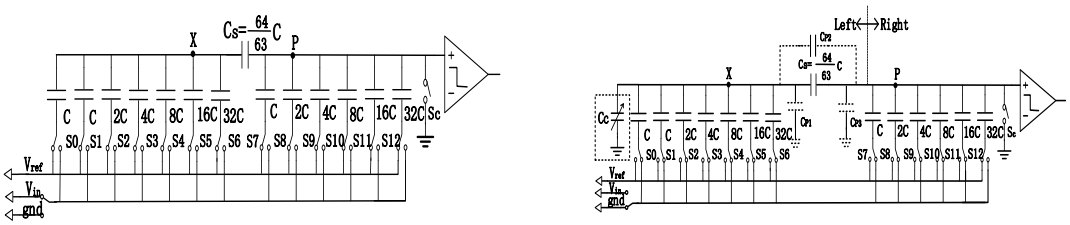
When all the capacitors are connected V_{in} and the upper plate is grounded, DAC enters the sampling phase. At this point, the charge of node P is:

$$Q_p = -64C * V_{in} \tag{1}$$

Then the bottom plate of the capacitor is grounded and upper plate break with ground, where the output voltage of DAC V_p is equal to V_{in}. Then switch S_{12} connects V_{ref}, which lead the circle into redistribution phase of the charge. At this time the voltage of point P :

$$V_p = -V_{in} + \frac{1}{2}V_{ref} \tag{2}$$

If V_p is larger than 0, it means that $V_{in} < \frac{1}{2}V_{ref}$, where the comparator output is high level; if V_p is smaller than 0, the comparator output is low level. Then V_{in} will respectively compare with $\frac{1}{4}V_{ref}$, $\frac{3}{4}V_{ref}$,and so on$\cdots$, until the end of the compare between last bit in the logical control and V_{in}.



(a) The traditional 12bit split CDAC circuit （b）A 12bit split CDAC circuit with calibration

Fig. 2 The circuit of 12bit CDAC

Since the capacitance value of the split capacitor is not an integral multiple of the unit capacitance, DAC will introduce a capacitance error value C_{p2}. At the same time, on the left and right sides of the capacitor array on the plate will also generate the node capacitance C_{p1} and C_{p3}. The three error capacitances greatly reduce the conversion accuracy and linearity of the DAC, therefore, in this paper, an self calibration method is proposed to eliminate the error caused by the above problems. As shown in Fig. 2 (b), the part of capacitance C_c is self calibration circuit. When the C_c do not be considered, the error caused by C_{p1}, C_{p2} and C_{p3} mainly occurred in the sampling stage. So switch of S_0~S_{12} connect V_{in} and switch of S_c is grounded. The voltage of point X is the partial pressure of V_{in} at X:

$$V_x = \frac{64C}{64C + C_{p1} + C_s + C_{p2}} \cdot V_{in} \tag{3}$$

Calculate equivalent capacitance the left of P:

$$C_{eq\_L} = \frac{(C_s + C_{P2}) \cdot 64C}{64C + C_{P1} + C_s + C_{P2}} \tag{4}$$

At this time, the high 6 bit capacitor on the right side of P connect V_{in}, and parasitic capacitance C_{p3} is grounded at both ends. Therefore, the total charge of P in sampling stage for savings:

$$\begin{aligned} Q_{p\_sample} &= C_{eq\_L} \cdot (-V_{in}) + 63C \cdot (-V_{in}) \\ &= -(C_{eq\_L} + 63C) \cdot V_{in} \end{aligned} \tag{5}$$

By formula (4), formula (5), because of the influence of C_{p1}, C_{p2} that he equivalent capacitance on the left of P deviate from the unit capacitance when sampling, there will be sampling error. If $C_{eq\_L} = C$, the sampling error can be eliminated where the total charge of P can achieve $-64C \cdot V_{in}$.

In the X point access to a adjustable C_c, it is parallel with the C_{p1}.Assumption P look left equivalent capacitance is C_{eq_L1}, then the C_{eq_L1} expression is as follows：

$$C_{eq\_L1} = \frac{(C_s + C_{P2}) \bullet 64C}{64C + C_{P1} + C_c + C_s + C_{P2}} \tag{6}$$

Make C_{eq_L1} equal to the unit capacitance, the value of the calibration capacitor can be obtained from the formula (6):

$$\begin{aligned} C_c &= 63C \cdot (C_s + C_{P2}) - 64C - C_{P1} \\ &= 63C_{P2} - C_{P1} = \left(2^k\text{-}1\right) \cdot C_{P2} - C_{P1}, k = 8 \end{aligned} \tag{7}$$

where k is the number of capacitors on the left. The sampling error can be eliminated from the formula (7) , but the calibration capacitor also has an effect on charge redistribution. First of all, the sampling phase ends up in the hold phase. When S_0~S_{12} is grounded, the S_c is disconnected, then the equivalent capacitance on the left of P is as follow:

$$C_{eq\_q} = (64C + C_{P1} + C_c) // (C_s + C_{P2}) = C + \frac{63C_{P2}}{64} \tag{8}$$

The voltage of P:

$$V_{p\_hold} = -\frac{64C}{64C + \frac{63C_{P2}}{64} + C_{P3}} V_{in} \tag{9}$$

In charge redistribution phase, the potential of P is the sum of partial pressures of V_{p_hold} and V_{ref} :

$$\begin{aligned} V_P &= -\frac{64C}{64C + \frac{63C_{P2}}{64} + C_{P3}} V_{in} \\ &+ \frac{64C}{64C + \frac{63C_{P2}}{64} + C_{P3}} \cdot \frac{1}{2^k} V_{ref} \\ &= \frac{64C}{64C + \frac{63C_{P2}}{64} + C_{P3}} (-V_{in} + \frac{1}{2^k} V_{ref}) \end{aligned} \tag{10}$$

Drawn from the above calculation, the calibration capacitor can be completely eliminated in nonlinear circuit distortion, but when the sampling stage is completed, a capacitance error is introduced in the left of P, which has the value of $63C_{p2}/64$. Finally, a factor of less than 1 is introduced when the comparator input voltage V_p is generated. Increasing the gain of the comparator can counteract this factor, which has little effect on the normal operation of the ADC.The logic control part of the calibration circuit is shown in Fig.3, where C_c is a binary weighted form of calibration capacitance. The calibration process of DAC is as follows:
Connect S_0~S_6 to V_{ref} , and S_7 is connected to the ground with the switch S_c is closure. Charging for P, then the charge of p:

$$Q_P = V_{cm}(C + C_e) - C_{eq\_L} \cdot V_{ref} \tag{11}$$

Then switch S_0~S_6 is connected to the ground, and switch S_c is off with the switch S_7 connected to V_{ref} . The output voltage of p:

$$V_P = \frac{V_{cm}(C + C_{eq\_L1}) - C_{eq\_L1} \cdot V_{ref}}{C + C_{eq\_L1}} + \frac{C \cdot V_{ref}}{C + C_{eq\_L1}} = V_{cm} + \frac{C - C_{eq\_L1}}{C + C_{eq\_L1}} V_{ref} \tag{12}$$

By comparing the value of V_p and V_{cm} in the comparator, the result of the comparator output to the logic control part, then adjust the value of C_c , until the two voltages is equal.

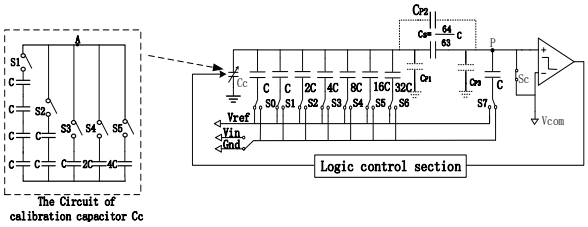
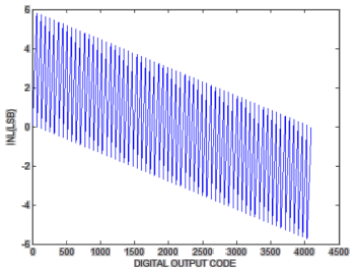


Fig.3 The circuit of DAC calibration

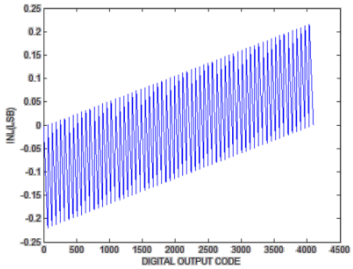
The formula (7) shows that the value of adjustable capacitor C_c for calibration consists entirely of parasitic capacitance C_{p1} and split capacitor error C_{p2} , relative to the effect on the error of the expanded 2^k-1 times. Without calibration, it is very difficult to control the equivalent capacitance of the segmented capacitor and the capacitance array of the left side by the traditional layout design.

III. SIMULATION RESULTS

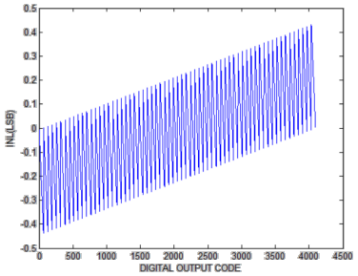
At the current technology, C_{p1} is generally not greater than 1C, and C_{p2} is not greater than 0.1C. Here it assumes worst case where C_{p1} is 1C and C_{p2} is 0.1C. The figure of INL (Integral Non-linearity, integral nonlinear error) by MATLAB is shown in Fig.4.



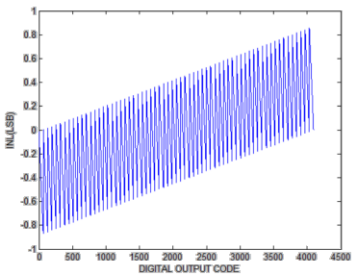
(a)The INL value without calibration



(b)The INL value of the calibration circuit with step length of 0.25C



(c)The INL value of the calibration circuit with step length of 0.5C



(d)The INL value of the calibration circuit with step length of 1C

Fig. 4 The change of INL value caused by the step size of the calibration circuit

The INL values without adding calibration are shown in Figure 4 (a), where the value is around ±6LSB. Individually adding a calibration circuit with the step size of 0.25C, 0.5C and 1C, then the INL value is as shown in Fig4 (b), (c) and (d). When the step size of is 0.5C, the INL value dropped to ±0.42LSB which has

been less than ±0.5LSB. At this time, the performance has meet the requirements of circuit design. But this value is easily affected by external environment.So the circuit selects the step size of the 0.25C, and the INL value is ±0.22LSB.The calibration circuit of step length is designed to 0.25C, which is the trade off between the number of unit capacitors and the resolution requirements.The simulation of ADC using Spectre simulation tool in Cadence software, input signal is sine wave with the frequency of 30Hz, and frequency of sampling circuit is 7.8kHz. Sampling points of the simulation results of Cadence is 4096, the frequency spectrum of data by MATLAB is as shown in Fig.5.

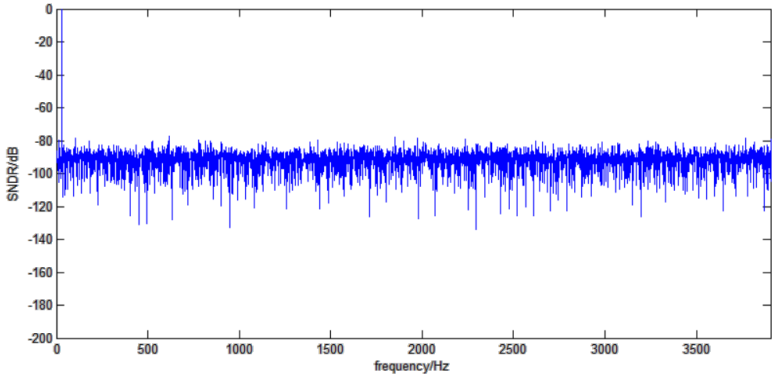


Fig. 5 The output spectrum of SAR ADC after calibration

Fig.5 shows that the SNDR reaches 71.47dB with the circuit utilizing calibration, and the effective bits reach 11.51bit. From Table.1, compared with paper [1], this paper not only increases the resolution of ADC, while reducing the power consumption of the circuit. When it comes to paper [7], the ENDR and INL value in this paper are closer to the design precision, and calibration circuit is stronger to eliminate the nonlinear error.

Table.1 Simulation and comparison

	Paper[1]	Paper[7]	This work
Technology	65nm	0.13□ m	0.13□ m
Supply voltage	1.2V	0.5V	1.2V
Resolution	8bit	11bit	12bit
Power consumption	1.83mW	730nW	26□ W
SNDR	45.7dB	5.5dB	71.47dB
ENDR	7.3bit	9.93bit	11.51bit
INL	-0.3/+0.3LSB	-1.47/+1.83LSB	-0.25/+0.25LSB

IV. CONCLUDING

This paper introduces the design of a self calibration with split capacitor charge redistribution DAC 12bit SAR ADC by technology of CMOS 0.13μm. The self calibration method based on split charge divided type DAC circuit is added in the form of binary weighted adjustable capacitor array, which eliminates the parasitic electric capacity and nonlinear error caused by capacitor mismatch effectively. The effective number of ADC reached 11.51*bit*, and the INL value is controlled within -0.25~+0.25LSB, the overall power consumption is only 26μW. *C*ompared with other paper, this work achieves higher precision and lower power consumption.

V. ACKNOWLEDGEMENTS

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