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Voltage sag mitigation in distribution line by using DVR

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***Abstract*—**This proposed controller supplements the voltage-sag compensation control of the DVR for downstream fault current interruption in a radial distribution line . It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated pharos parameters, and this enables effective fault current interrupting even under arcing fault conditions. The results of the simulation studies performed in the PSCAD/EMTDC software environment indicate that the proposed control scheme: 1) can limit the fault current to less than the nominal load current and restore the point of common coupling voltage within 10 ms; 2) can interrupt the fault current in less than two cycles;3) limits the dc-link voltage rise and, thus, has no restrictions on the duration of fault current interruption; 4) performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions.

Key Words*—Digital filters, dynamic voltage restorer (DVR), fault current interrupting, multiloop control.*

I. INTRODUCTION

The dynamic voltage restorer (DVR) is a custom power device utilized to counteract voltage sags. It in-jests controlled three-phase ac voltages in series with the supply voltage, subsequent to a voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle. shows the main components of a DVR (i.e., a se-ries transformer, a voltage- source converter (VSC), a harmonic filter, a dc-side capacitor and an energy storage device. The line-side harmonic filter consists of the leakage inductance of the series transformer and the filter capacitor. The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current [9]–[11]. also to limit or interrupt the downstream fault currents. A control approach to enable a DVR to serve as a fault current limiter is provided in . The main drawback ofthis approach is that the dc-link voltage of the DVR increases due to real power absorption during fault current-limiting operation and necessitates switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of as low-decaying dc fault current component using the methods introduced in [7] and[12].To overcome the aforementioned limitations, this paper proposes an augmented control strategy for the DVR that provides:1) voltage-sag compensation underbalanced and unbalanced conditions and

2)a fault current interruption (FCI) function. The former function has been presented in [13] and the latter is described in this paper.

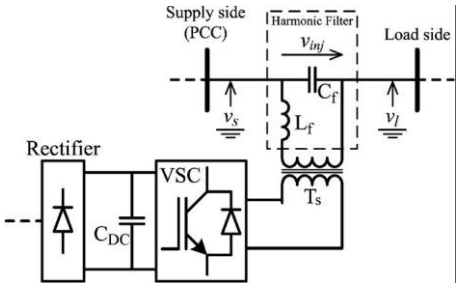

Fig. 1. Schematic diagram of a DVR with a line-side harmonicfilter.

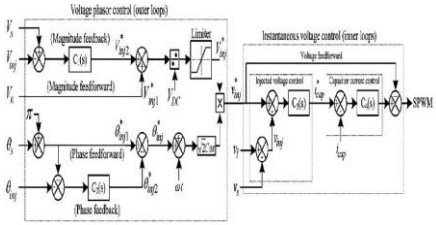

Fig. 2. Per-phase block diagram of the DVR control system in FCI mode.

The performance of the proposed control scheme is evaluated through various simulation studies in the PSCAD/EMTDC platform. The study results indicate that the propose control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective

fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions.

1. Voltage Phasor Control System

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase opposition [i.e., the injected phasor is controlled to be]. Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback

control system [17], [18], [21]–[27]. Fig. 2 shows two proportional-integral (PI) controllers (and) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller.

2. Instantaneous Voltage-Control System

Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor-based controller is directly fed to the sinusoidal pulse-width modulation(SPWM)unit. However, resonances of the harmonic flter cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances. The generated reference signal for the injected voltage is compared with the measured injected voltage ,and the error is fed to the voltage controller. As shown in Fig. 2, the output of the voltage controlleris the reference signal for the filter capacitor current control loop. It is compared with the measured capacitor current, and the error is fed to the current

controller. The steady-state error of the proposed control system is fully eliminated by the PI controllers in the outer control loop (i.e., and), which track dc signals (magnitude and phase angle).Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. and are pure gains and ,respectively.

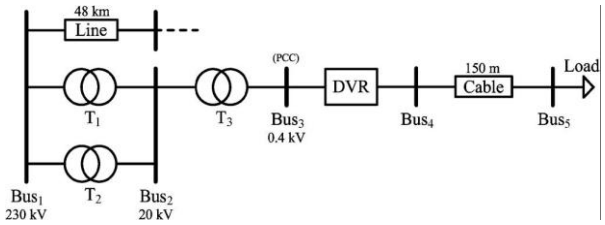

Fig. 3. Single-line diagram of the system used for simulation studies.

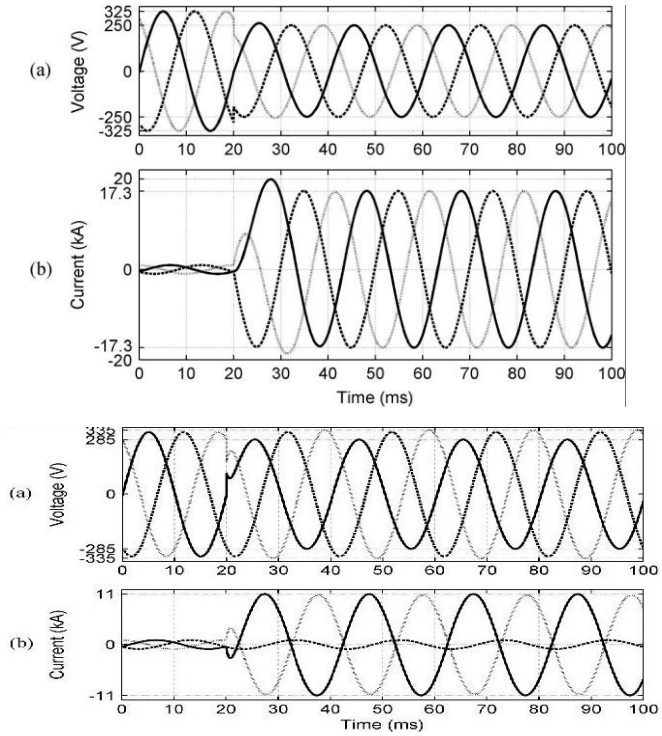

Fig. 5. (a) Voltages at . (b) Fault currents, during downstream three-phase fault when the DVR is inactive (bypassed).

PROPOSED FCI CONTROL STRATEGY *A.*

Three-Phase Downstream Fault

The system is subjected to a three-phase short circuit with negligible fault resistance at t=20msat.Priortothefaultinception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by thieve). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to17 times the rated load current (Fig. 5). Fig. 6 shows FCI performance of the proposed DVR control system during the fault. Fig. 6(a)–(c), respectively, shows the three-phase injected voltages, the restored three-phase supply-side voltages, and the three-phase load-side voltages which are reduced to zero to interrupt the fault currents. The slightly injected voltage by thieve before the fault initiation [Fig. 6(a)] is the voltage across the series impedance of the DVR series transformer secondary winding.Fig. 6(d) shows the line currents (i.e., the currents passing through the DVR). Fig. 6(d) illustrates that the proposed FC method limits the maximum fault current to about 2.5 times the nominal value of the load current and interrupts the fault currents in less than 2cycles. Fig. 6(e) depicts variations of the dc-link voltage during the FCI operation, and indicates that the dc-link voltage rise under the worst case (i.e., a severe three-phase fault) is about 15% and occurs during the first 5 ms after fault inception.

B. Phase-to-Phase Downstream Faults

The system of Fig. 4 is subjected to a phase-A to phase C fault with the resistance of 0.05at 10% of the cable length connecting to ,at 20ms. When the DVR is inactive (bypassed) during the fault(Fig. 7), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11times the rated load current. Fig. 8 illustrates that when the DVR is in service, the pro-posed FCI control successfully interrupts the fault current and

Fig. 7. (a) Voltages at , (b) Fault currents, during downstream phase-to phase fault when the DVR is inactive (bypassed).

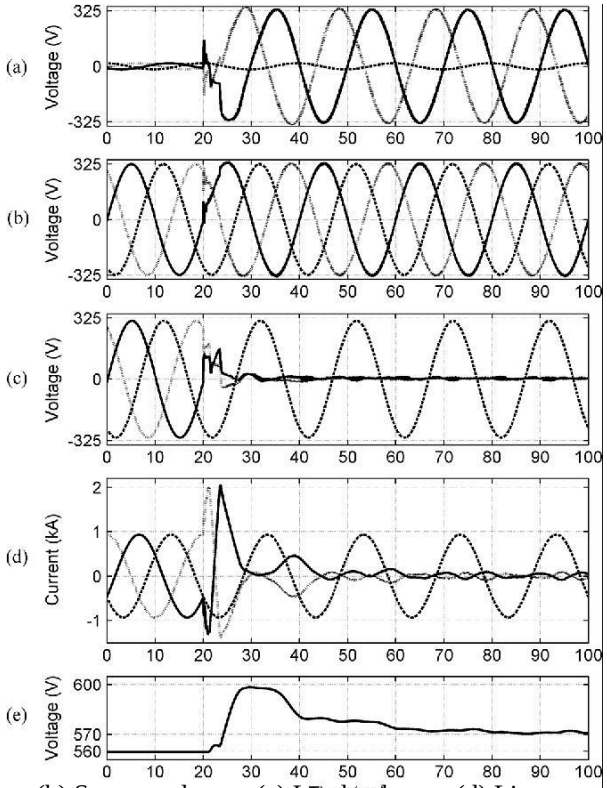

Fig. 6. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the three phase downstream fault.

Fig. 8. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the phase-to-phase downstream fault.

restores the PCC voltage of the faulty phases within two cycles. Fig. 8(e) shows that the dc-link voltage rise is less than 7%.Fig. 8 also shows that only the two faulty phases of the DVR react, and the healthy phase is not interrupted.

C. Single-Phase-to-Ground Downstream Fault

Phase-A of the system of Fig. 4 is subjected to a fault with resistance of 0.2at 10% length of the cable connecting to ,at 20ms. If the DVR is inactive (Fig. 9), the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted the DVRto prevent possible damages to the VSC before this interrupted by the relays. The reason is that the operation time of the over current relays is considerable for a fault current of about 2.5 p.u.

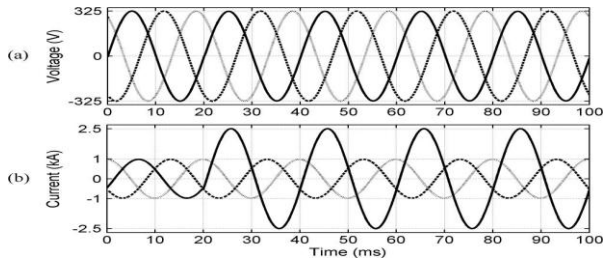

Fig. 9. (a) Voltages at . (b) Fault currents, during the downstream single phase-to-ground fault when the DVR is inactive (bypassed).

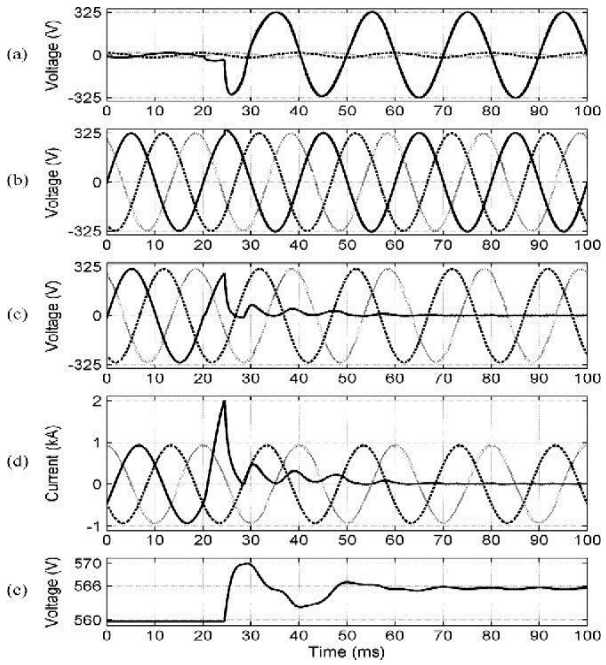

Fig. 10. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground down stream fault.

It must be noted that to prevent operation of three phase induction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such conditions and disconnect the load when any of the phases is de-energized by the single-phase operation of the FCIfunction. Furthermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the operator can decide either to use or disable this function depending on the type of load.

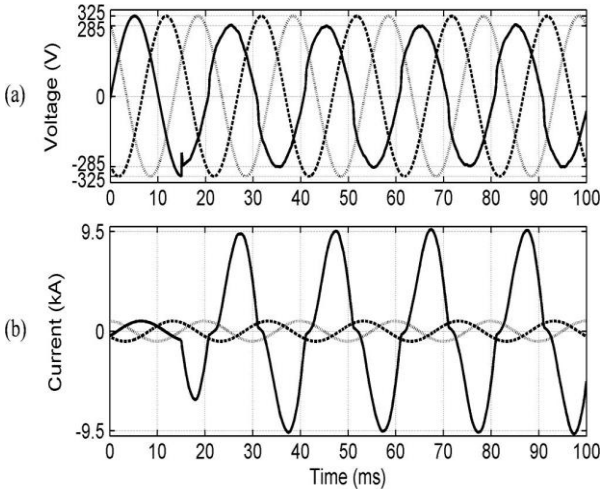

Fig. 11. (a) Voltages at . (b) Fault currents, during the downstream single phase-to-ground arcing fault when the DVR is inactive (bypassed).

D. Effect of the Fault v-i Characteristic

Due to the nonlinear v-i characteristic of a free-burning arc, the voltage and current waveforms are highly distorted during an arcing fault. To investigate the effects of such distortions on the performance of the proposed FCI control scheme, a single-phase-to-ground downstream arcing fault at considered.The arc is modeled based on the modified Cassie–Mayr equations [28]. The effect of variation of the arc length on the arc

voltage [29] is also taken into account.

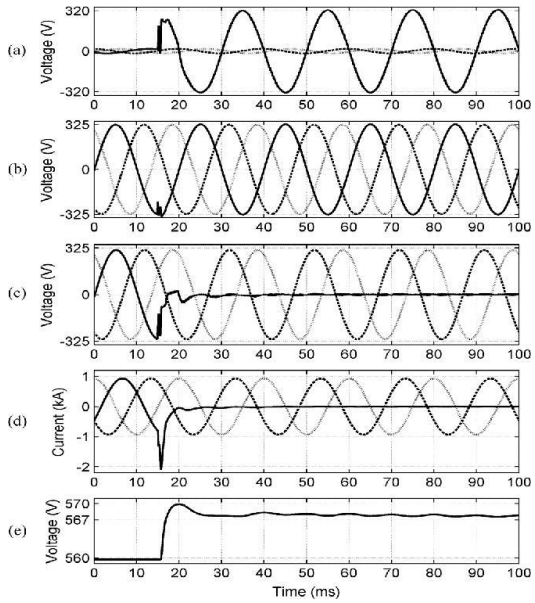

Fig. 14. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground down stream arcing fault.

E. Simultaneous FCI Operation and Sag Compensation

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At15 ms, the system of Fig. 4 is subjected to a phase-A to phase-B fault with the resistance of 1at 90% of the line length from. The fault causes 87% voltage sag at the PCC. At55 ms, another fault with the resistance of 0.2 on phase-A at
10% length of the cable connecting to occurs. The upstream fault is cleared by relays at t=93ms.

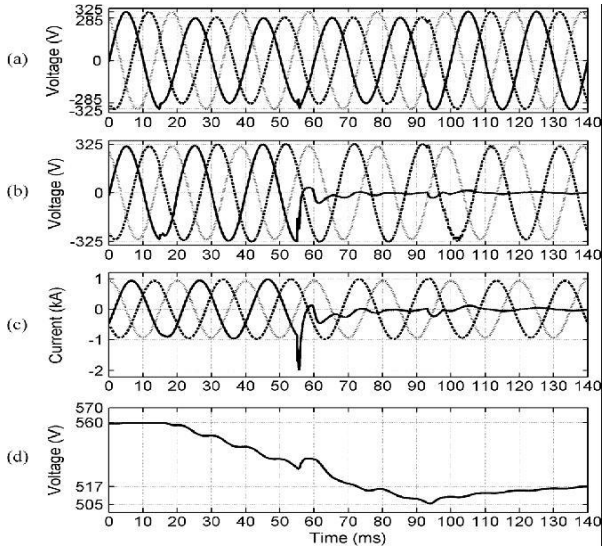

Fig. 15. (a) Source voltages. (b) Load voltages. (c) Line currents. (d) DC-link voltage, during phase-A to ground downstream fault which takes place during sag compensation in phases A and B.

Fig. 15(d) depicts variations of the dc-link voltage and indicates that the dc-link voltage drops during sag compensation, but the FCI operation maintains the dc-link voltage when it is lower than a certain value (the dc-link voltage, which is needed to reduce the load voltage to zero). This continues until the capacitor voltage approaches the aforementioned threshold. The reason is that when the capacitor voltage is lower than a certain value, the magnitude of the voltage injected by the DVR, which must be 180out of phase with respect to the

source voltage, is less than the source voltage magnitude. Thus, small current flows through the DVR until the capacitor is charged. This current results in active power absorption by the DVR.

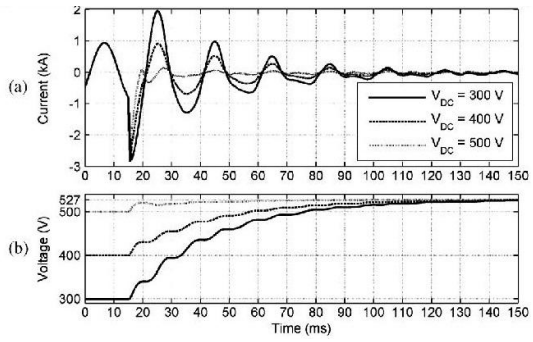

Fig. 16. (a) Line current of phase-A and (b) dc-link voltage, for different initial values of the dc-link voltage, during downstream phase-A-to-ground fault.

II. CONCLUSION

This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. This control function is an addition to the voltage-sag compensation control of the DVR. The performanceOf the proposed controller ,under different fault scenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in thePSCAD/EMTDC environment.The study results conclude that:The proposed multi loop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter; The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz); The proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, tolessthan15%andenablestheDVRtorestore
The PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltage conditions. The proposed control system also performs satisfactorily under downstream arcing fault conditions.

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