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Tenso properties of field-effect transistors in channel cutoff mode

A.V. Karimov, D.R. Djuraev, O.A. Abdulhaev, A.Z. Rahmatov,
D.M. Yodgorova, A.A. Turaev

Physical Technical Institute, SPA "Physics-Sun", Academy of Sciences of Uzbekistan. 100084, Tashkent, Bodomzor Yuli Street, 2b;

Abstract: There are presented the results of experimental investigation of sensitivity of field effect transistor in bipolar mode connection with cutoff channel to the impact of pressure and light exposure. It is shown that the field effect transistor in bipolar mode has a high sensitivity to pressure.

Keywords*: field-effect transistor, pressure sensor, falling voltage, cutoff mode*.

I. INTRODUCTION.

The growing interest to micro-power [1] semiconductor devices manifested by professionals in the field of radio electronics, information display and optoelectronics is conditioned due to their excellent features: low power consumption, reliability, long life and high stability of their parameters. From this point of view, field-effect transistors having a wide range of connection modes are highly demanded.

In particular, for creation of structures with the maximum sensitivity are required FETs with the depth of p-n-junction, commensurated with the depth of penetration of the light radiation [2], and a special selection of the channel thickness will allow to give to structure the temperature sensitivity. Here the positive sign of the temperature sensitivity coefficient is formed due to the dependence of contact potential difference of p-n-transition from temperature, and a negative temperature coefficient sign - owing to dependence of the mobility of charge carriers in the channel from the temperature [3].

The present work is devoted to the study of tenso properties of silicon field-effect transistor with p-n-junction in the blocking mode, in particular, to ensure sensitivity to external influences such as pressure. To reach this our goal it is necessary to choose a universal parameter correlated with the region that responds to all these influences.

We have chosen as such a parameter cut-off voltage interconnected with the area of space charge and located between channel and gate region whose thickness is controlled by the source-gate junction potential while potential itself is created by voltage of transition drain-gate. The proposed choice is conditioned due to the many physical processes, like generation of minority carriers, change in capacitance, height of potential barrier are associated with the dynamics of the space charge location change.

1. Experimental Samples

The investigated silicon junction field-effect transistor shown in Fig. 1a contains a low-resistance substrate of p-type with the bottom gate electrode and a high-resistance epitaxial n-type layer grown on the surface of substrate. Further on the surface of epitaxial layer formed ohmic contacts to drain and source regions, between which a channel is located.

The carrier concentration in the substrate and the channel is $1.0 \cdot 10^{19}$ cm^{-3} and $2 \cdot 10^{15}$ cm^{-3}, respectively.

The thickness of the channel is 1 μm, and length is 50 μm.

The investigated structures have a typical field-effect transistor sub-linear current-voltage characteristics with the maximal drain current of 1.8÷2.2 mA and the pinch-off voltage of 0.9÷1.3 V, Fig. 1b.

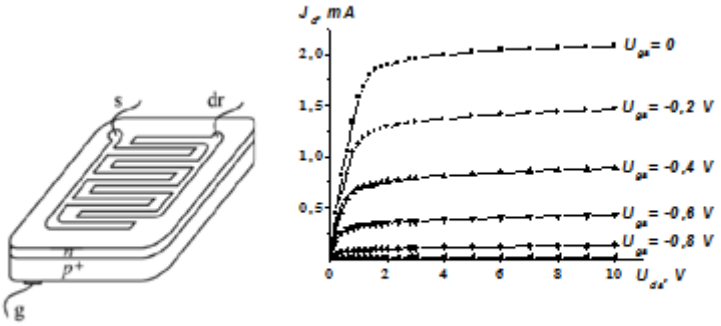

Fig.1. Geometric design (a) and current - drain voltage characteristics (b) of the FET.

2. Experimental Techniques

The electric circuit designed for direct measurement of the pinch-off voltage drop at the source-gate junction is shown in Fig. 2.

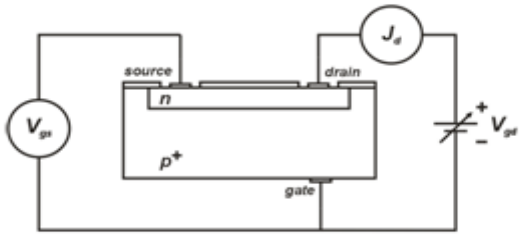

Fig. 2. Field-effect transistor connection circuit to study external influence

Power supply unit is connected to the drain-gate junction via microamperemeter. Herewith the potential generated at the source-gate junction is fixed by the second voltmeter. As the drain voltage increases until the reach of pinch-off voltage, the voltage drop at the source increases linearly, and when the channel is pinched-off by the space-charge layer it becomes equal to the pinch-off voltage and is maintained at this level.At a given work voltage impact on the channel of any factor (pressure, light or temperature) leads to a changing of source-gate junction potential, which is identified as mentioned above like the measuring parameter.Under illumination of channel in space charge region are generated electron-hole pairs which created photocurrent on the source-gate junction leading to the decreasing of resistivity of this junction that in turn causes to the decreasing of voltage drop and relevant increasing of current of the gate-drain.

3. The Sensitivity to Pressure of the Depletion Mode Field-Effect Transistor

As shown in Fig. 3, studies have demonstrated that under the external pressure the voltage falling at the gate-source junction (pinch-off voltage) linearly decreases. Increasing of pressure from 0.027 g/cm^2 to 0.26 g/cm^2 leads to decreasing of pinch-off voltage from 1.2 to 0.86 V.

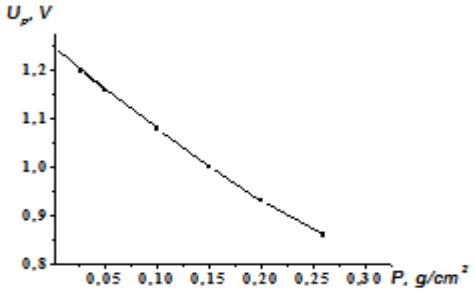

Fig. 3. Dependence of pinch-off voltage from pressure

Thus, the coefficient of pinch-off voltage sensitivity to pressure (tenso-sensitivity)

$$\alpha_P = (U_P^2 - U_P^1) / (p_2 - p_1) \qquad (1)$$

amounts 1.46 V/(g/cm^2) or 1.46·mV/Pa, which is two orders of magnitude higher than the stress sensitivity of the collector junction of a known bipolar transistor [4].

The observed decrease of pinch-off voltage of the channel with pressure growing can be explained by decreasing of the band gap of material of channel from pressure and increasing of dielectric permittivity of the material of the channel, which as seen from Eq. (2) leads to increasing of initial thickness of the space charge region of p-n-junction of the gate

$$W_{SCR} = \sqrt{\frac{2\varepsilon\varepsilon_0 U_{diff} (N_{chan} + N_{gate})}{q \cdot N_{chan} \cdot N_{gate}}} \qquad (2)$$

that leads to a reduction of the thickness of channel's conducting part.

So, the increasing of pressure on the surface of the channel leads to even lower voltage for its pinch-off[5]:

$$U_P = \frac{N_{chan} qa^2}{2\varepsilon\varepsilon_0}\left(1 + \frac{N_{chan}}{N_{gate}}\right) = U_{rev} + U_{diff} \ . \qquad (3)$$

Accordingly, dependence of the thickness of depletion layer from the reverse voltage can be determined by the following expression [5]:

$$W_{SCR} = \sqrt{\frac{2\varepsilon\varepsilon_0 (U_{diff} + U_{rev})(N_{gate} + N_{chan})}{qN_{gate} N_{chan}}} \ . \qquad (4)$$

In Eq. (2) and (4): ε and ε_0 - permittivity of semiconductor and vacuum, respectively; U_{rev} - voltage applied to the p^+-n-junction of the gate; N_{gate} - and N_{chan} - charge carrier concentration in low-resistant gate and high-resistant channel regions; q - charge of electron.Thus, one can conclude that with increasing pressure on the channel the thickness of the channel's conducting region is reduced that, in turn, decreases of pinch-off voltage.

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