A Comparative Study of Electrical Properties of Si and ZnO Gate-all-around Nanowire FET

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Abstract:- A comparative study of various electrical properties of n-channel Si And ZnO Gate-all-around (GAA) nanowire Field-Effect Transistors has been assessed and presented. The simulation results shown here are found on the basis of self-consistent solution of energy balance equation. The temperature, channel diameter and gate length dependence of various electrical parameters like subthreshold swing (SS), threshold voltage and transconductance have been simulated. ZnO nanowire FET showed better threshold voltage but poor subthreshold swing and transconductance with respect to Si nanowire FET.

Keywords: *GAA, Si, ZnO, Nanowire FET, SS, Threshold voltage, Transconductance*

I. INTRODUCTION

In modern electronic circuits, transistors have been implemented as basic modeling elements. For the past few decades, MOS devices have been developed at a dynamic pace [1]. From Moore's law, dimensions of transistors have been reduced to nanoscale. Although varying of dimensions affects information processing system of transistors, it might cause few technical problems [2]. Gate-all-around (GAA) FET is advantageous over FinFET and silicon-on-insulator (SOI) technology as it overcomes the problem of mobility loss due to channel width variations. GAA FET is a nanowire structure where the gate surrounds all the four sides of the channel. This structure enables the transistor to obtain good gate control over the channel which is very much integral for building next generation nanowire transistors. The knowledge of working methods of solid state devices is indispensable for device physics. Simulation is becoming very much important for understanding different process parameters of NWTs. Simulation tools can assist experimental work to modify the FETs [3], minimize their cost, point out their pros and cons, and demonstrate their scalability down to the nanometer range [4-5].

II. NEED AND SCOPE OF PRESENT STUDY

ZnO is touted as one of the most pre-eminent II-VI semiconductors that have been investigated since the early 1930s [6-7]. ZnO is a direct bandgap material having a bandgap of about 3.4eV [8]. It crystallizes in the hexagonal wurtzite type structure [8]. ZnO has become an alluring choice for transparent conductors and FET as it has large bandgap and possibility of introducing n type dopants is also there [9]. The bandgap modulation over wide range by alloying cadmium and magnesium has been demonstrated for UV-optoelectronics [6]. Nanoparticles and nanowires of ZnO have been implemented as electron transport layer in dye-sensitized solar cell [10-11]. Development of 1-D ZnO nanostructures as biosensors is in the initial but potential stage [12-17]. Various enzymes have been deactivated in order to realize highly selective bioassays [18-20]. Surface modification of ZnO nanowires with biotin for streptavidin detection has been reported recently [21]. For uric acid detection, Enzyme coated ZnO nanowire FET have been used [22]. In literature, further ZnO nanowire use for DNA sensory applications can be observed [23]. There have been several studies focusing on the development of Si-NW sensors during the last decade due to availability and ease of fabrication [24-26]. Si-NWs are CMOS compatible [27]. But ZnO-NWs are not CMOS compatible but it works quite well under ambient conditions and oxygen rich environment [28-30]. The industry has reached the saturation limit and the need for better and efficient material for nanowire FET has increased greatly with the span of time. Thus ZnO can become a good alternative. In this paper, a comparative simulation based study of different parameters has been provided considering the importance and increasing demand of Si and ZnO nanowire transistors in different applications.

III. DEVICE CONFIGURATION AND SIMULATION METHODOLOGY

The device structure of Gate-all-around n-channel nanowire FET structure has been illustrated in Fig. 1, which consists of Oxide Thickness *Tox*, channel diameter *Dch*, gate length *Lg*, source length *Ls,* drain length *Ld,* gate overlap to source *Os,* gate overlap to drain *Od*. Further, the oxide is placed on either sides of the side walls of the FET. The thickness of the side wall oxide is specified by *tox*1 and *tox*2. For simulation purpose,

source and drain lengths were both chosen 100nm and the gate length has been varied in the range of 500 nm to 800 nm, channel diameter from 20 nm to 60 nm. The oxide thickness has been taken 10 nm and kept constant throughout the simulation studies. The drain and source doping has been kept fixed at 2×10^{24} cm^{-3} and channel doping was 8×10^{16} cm^{-3}. The gate bias was varied from -1.5 V to 2 V whereas drain bias has been kept at 0.8V. Oxide overlap has not been considered.
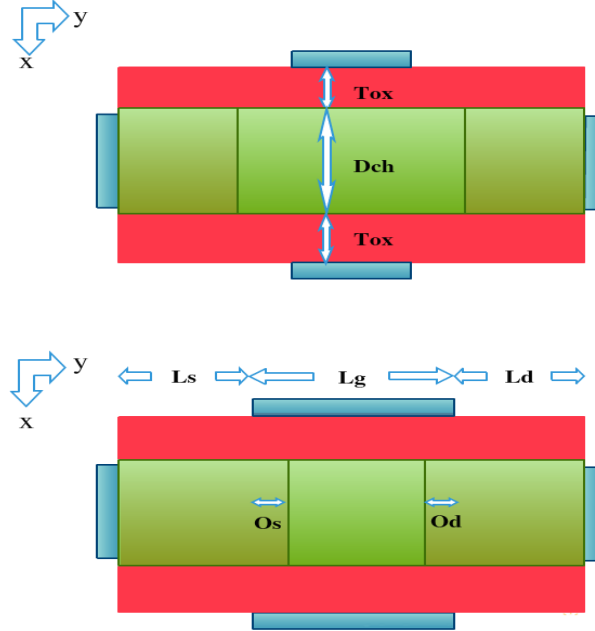

Fig. 1. Two Dimensional structure of Gate-all-around Nanowire FET device for geometry- x and for geometry- y [31]

A simulation tool named MuGFET was used to observe various effects of the nanowire parameters like temperature, gate length and channel diameter on NWT I_d–V_g characteristics. The MuGFET software was designed and developed at Purdue University. MuGFET is a software for simulating different electrical properties for nanoscale multi-gate FET structures [31]. From MuGFET, PADRE simulator was used which was developed at Bell Laboratories. PADRE is basically a device oriented simulator for 2D/3D device with arbitrary geometry. It delivers many plots which come useful for better understanding of device operation. MuGFET provides self-consistent solutions to the Poisson and drift-diffusion equations for the calculation of the characteristics of NWTs [32].

TABLE I. List of various properties of Si and ZnO channel materials at 300 K undertaken for simulation study

S. No.	Properties		Si	ZnO
1	Energy band-gap (eV)		1.12	3.37
2	Dielectric constant		11.7	8.49
3	Electron affinity (V)		4.05	4.35
4	Electron effective mass		$0.2m_o$	0.26
5	Light Hole effective mass		$0.16m_o$	$0.59m_o$
6	Heavy Hole Effective mass		$0.49m_o$	$0.59m_o$
5	Density of states effective mass	Electrons	$1.18m_o$	$0.29m_o$
		Holes	$0.81m_o$	$1.21m_o$
6	Electron mobility (cm^2/V-s)		1450	300
7	Hole mobility (cm^2/V-s)		500	5
8	Saturation Velocity (cm/s)	Electrons	1.0×10^7	2.24×10^7
		Holes	0.704×10^7	3.4×10^5

IV.   SIMULATIONS AND RESULTS

### A. I_d vs. V_g curves for ZnO and Si
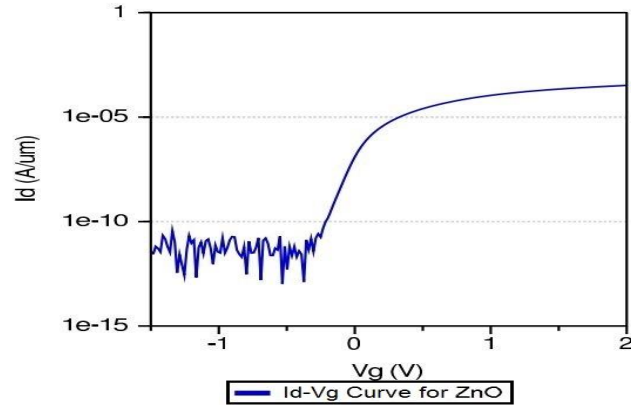
(a)
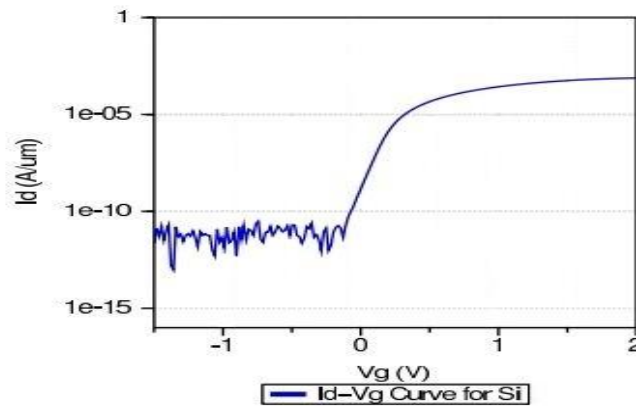
(b)

**Fig. 2.**   (a) I_d vs. V_g for ZnO   (b) I_d vs. V_g for Si

In fig. 2(a), it is shown that the normalized I_d-V_g graph for ZnO with moderately doped channel at 300K was simulated. It is observed from the graph that the on/off current ratio is about 10^6. The threshold voltage and subthreshold swing were found to be 0.394V and 113.891 mV/decade respectively. The simulation results were fairly in consonance with the experimental data for ZnO nanowire FET [33]. In fig. 2(b), the I_d-V_g graph for Si with moderately doped channel at 300K was shown. The gate length was chosen 800 nm and diameter was fixed at 60 nm for both ZnO and Si.

B. Subthreshold Swing vs. Temperature, Channel Diameter and Gate Length
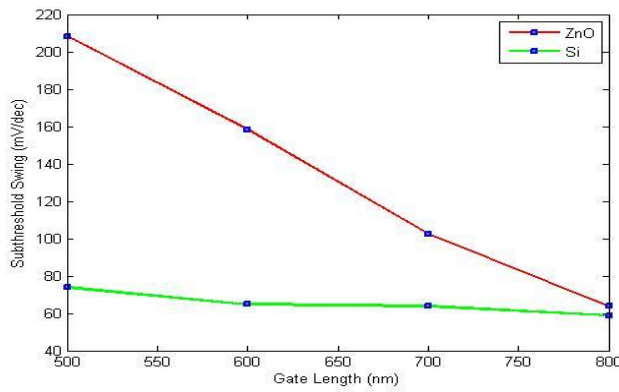
Subthreshold swing gives insight of the leakage currents associated with the device characteristics. Several studies suggest that subthreshold swing of ZnO nanowire FET being very high which complies with our result [33-34]. Small subthreshold swing means better channel control and improved I_{on}/I_{off} which usually means less leakage, and less energy.
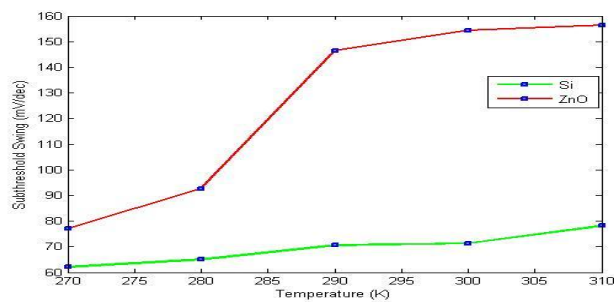

(a)
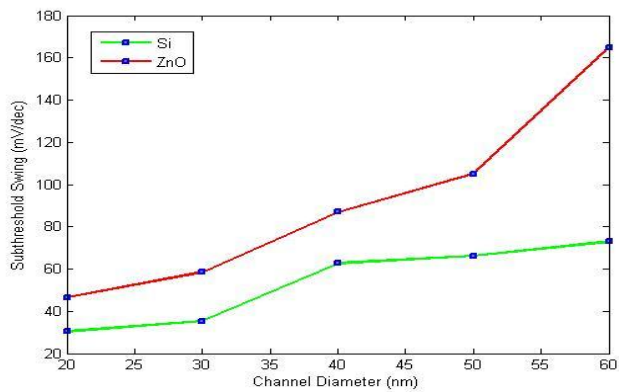
(b)

(c)

Fig. 3. (a) Subthreshold Swing vs. Temperature (b) Subthreshold Swing vs. Channel Diameter (c) Subthreshold Swing vs. Gate Length

In fig. 3(a), it has been observed that subthreshold swing increased with temperature as expected. At room temperature ZnO showed much worse subthreshold swing compared to Si. In fig. 3(b), subthreshold swing vs. channel diameter was plotted. The subthreshold swing increased for both Si and ZnO, ZnO showing the higher subthreshold swing. Similarly, in fig. 3(c), subthreshold swing vs. gate length was plotted. The subthreshold swing of Si was quite stable at all gate length whereas subthreshold swing of ZnO decreased steeply. At long gate length, ZnO and Si showed similar subthreshold swing.
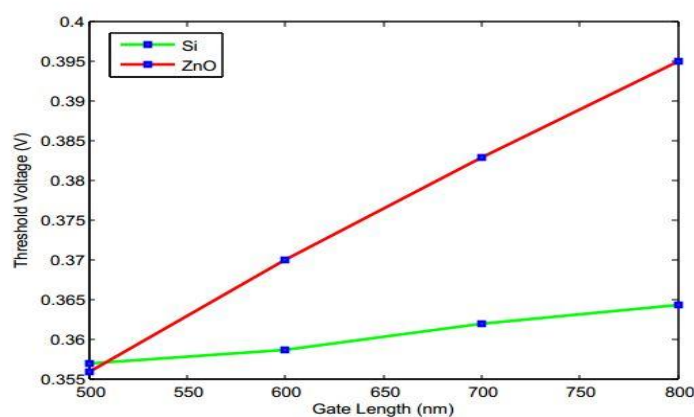
C. Threshold Voltage vs. Temperature, Channel Diameter and Gate Length
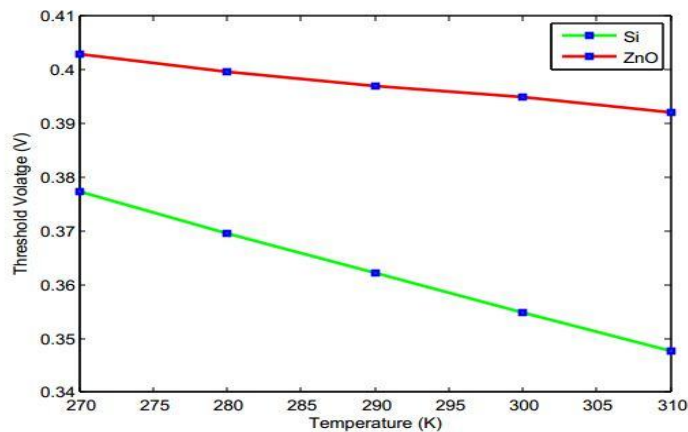
(a)
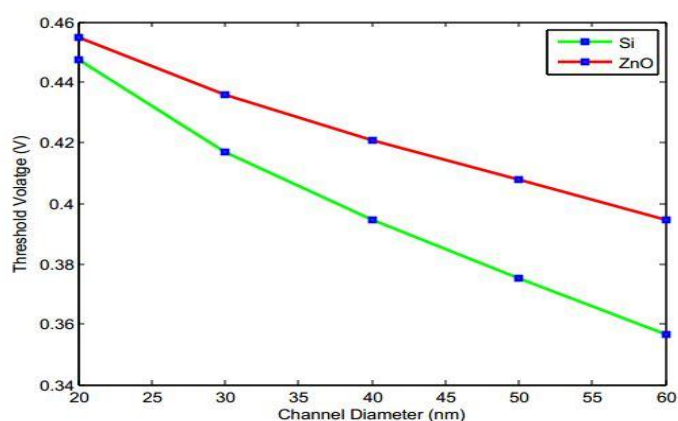
(b)

(c)

Fig. 4. (a) Threshold voltage vs. Temperature (b) Threshold voltage vs. Channel diameter (c) Threshold voltage vs. Gate length

The threshold voltage is a fundamental technological parameter that should be maintained properly for a nanowire device. In fig. 4 (a), by varying temperature from 270K to 310K, the decrease observed in threshold voltage in ZnO was found less steep than Si. ZnO provided higher threshold voltage than Si. In fig. 4 (b), this is also true for channel diameter while the diameter was varied from 20 nm to 60 nm. In fig. 4 (c), with the increase of gate length, threshold voltages increases. As the distance between the drain and source decreases, potential becomes more prone to drain electric field encroachment leading to an earlier threshold point of gate bias. Although the initial value for ZnO was lower than Si, the value of threshold voltage of ZnO increased very steeply with the increase of gate length. In all cases, Si offered worse threshold voltages. Lowering this threshold tends to result in the channel never being fully switched off – it's always leaking some current. From this perspective ZnO would be preferable for most logic application. However for low power device power efficiency is obtained by lowering threshold where Si would be useful.

D. Transconductance vs. Temperature, Channel Diameter and Gate Length

Transconductance, g_m, is a measure of the sensitivity of drain current to changes in gate-source bias. The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility for low drain voltages. In this simulation, ZnO has shown a lower transconductance with respect to Si which is obvious due to low electron mobility. So Si-NW FET are more sensitive than ZnO in this regard. In this simulation, normalized transconductance was plotted.
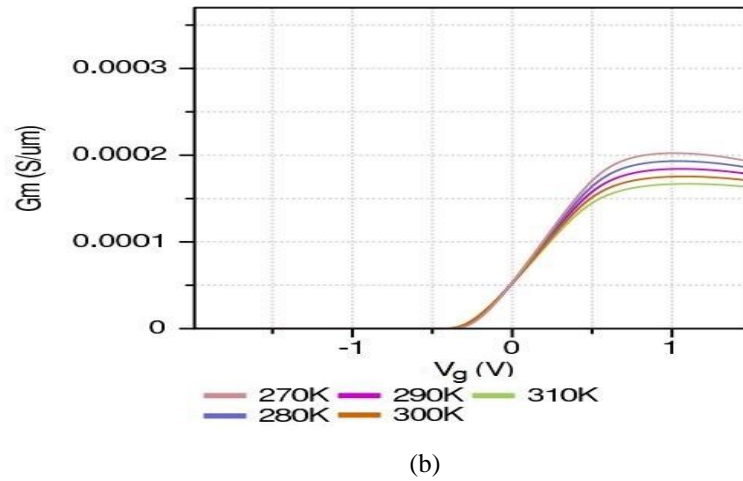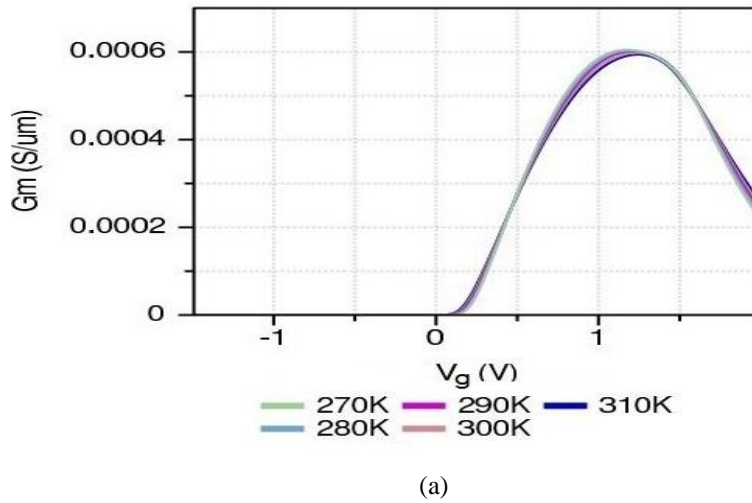
(a)

(b)

**Fig. 5.** (a) Transconductance vs. Temperature for Si   (b) Transconductance vs. Temperature for ZnO

In fig. 5(a), by varying temperature from 270 to 310K, it is observed that the highest transconductance for Si was achieved near about 1.2V. The transconductance for Si nanowire was quite stable. In fig. 5 (b), it is shown that for ZnO, highest transconductance was achieved near about 0.8V.

(a)
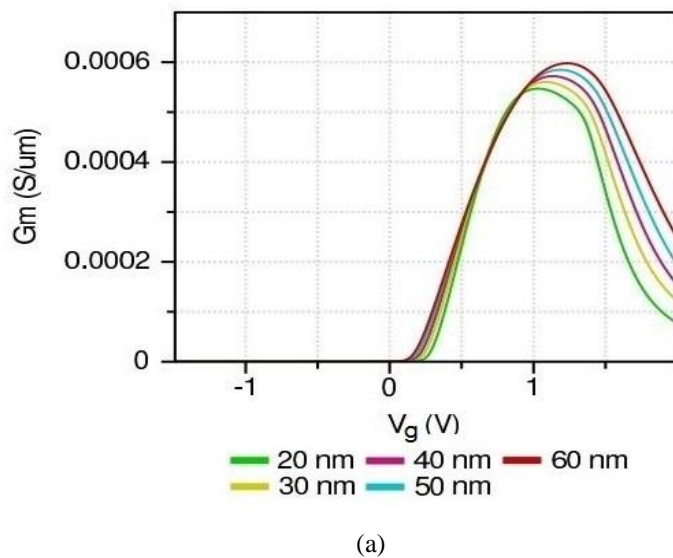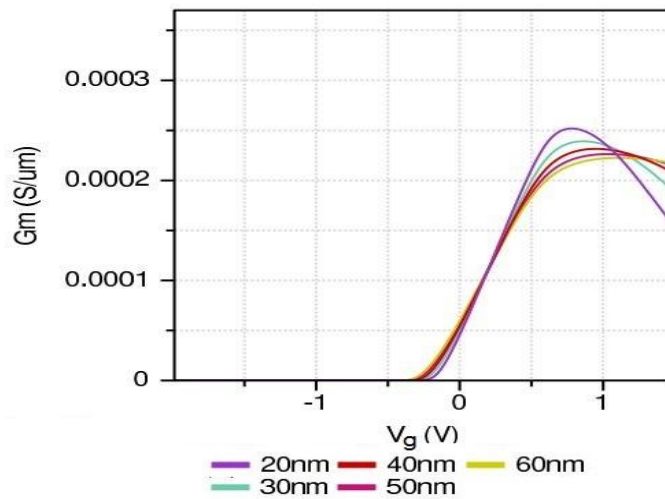
(b)

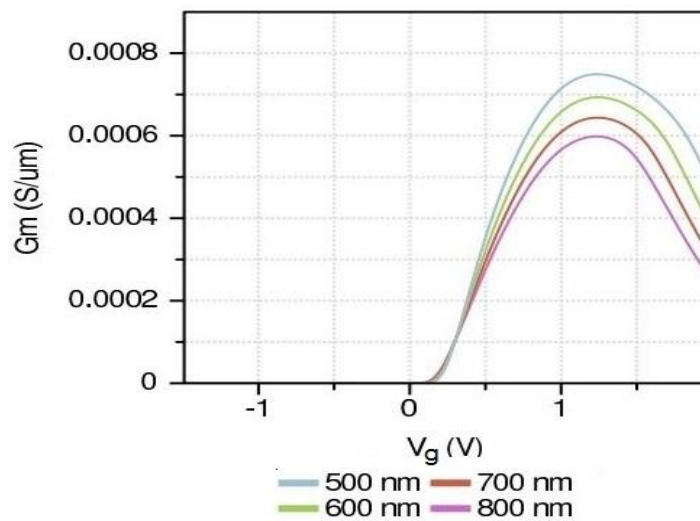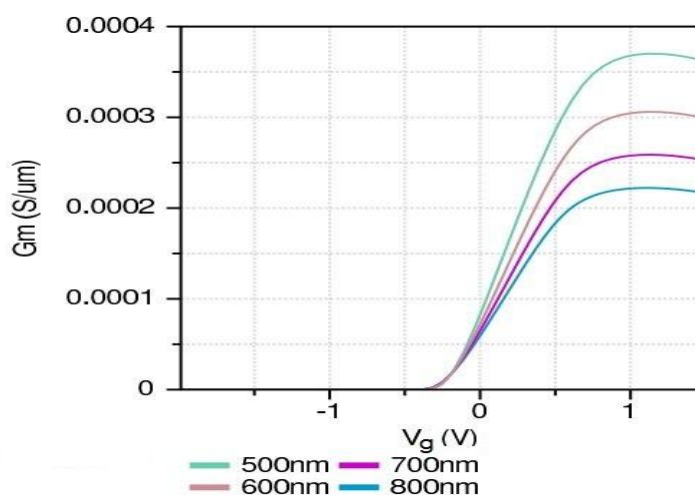**Fig. 6.** (a) Transconductance vs. Channel Diameter for Si (b) Transconductance vs. Channel Diameter for ZnO

In fig. 6 (a), it is shown that for Si, with the increase in channel diameter, the highest transconductance was increased and shifted to the right. In fig. 6 (b), it is shown that for ZnO, as the channel diameter increased, the highest transconductance decreased.

(a)

(b)

Fig. 7. (a) Transconductance vs. Gate Length for Si   (b) Transconductance vs. Gate length for ZnO

In fig. 7(a) and fig. 7 (b), with increase in gate length the transconductance for both nanowire FETs have decreased as expected [35]. Thus in all studies Si nanowire FET has shown higher transconductance than ZnO yielding higher gain and sensitivity.

V.   CONCLUSION

In this study, various electrical properties of ZnO and Si nanowire long channel FETs were analyzed. Properties like subthreshold swing, threshold voltage and transconductance study were observed by varying temperature, channel diameter and gate length keeping all other parameters constant. At room temperature, the subthreshold swing of ZnO surpassed that of Si by a large margin deteriorating the device performance. The subthreshold swing of ZnO improved a little with increasing gate length and lowering diameter. Hence to implement faster device Si is preferable. The threshold voltage of Silicon and ZnO varied less with temperature, channel diameter and gate length. ZnO showed better threshold voltage value than Si. So ZnO provides an attractive choice for logic applications. Again in case of transconductance, Si achieved better value than ZnO. For sensitive devices like biosensors, Si is still the better choice. ZnO has advantageous characteristics in the area of nano-biosensing and optoelectronics because of its stability in air, chemical stability, ease of synthesis and nontoxicity. But significant amount of research is yet to be done for improving the performance of ZnO nanowire FET. The main problem still being faced with ZnO nanowire FETs is a need for stable, reproducible p-type doping of ZnO which has not been achieved until now.

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