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Designing Of Low Power Sequential Circuits under Subthreshold Region Using Spadl and Gdi Techniques

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Abstract:–Low power design has become one of the primary focuses in both analogue and digital VLSI circuits. Many power consumption techniques have come in existence and with that the low power design is also achieved by scaling supply voltage, considering sub-threshold region in this region thereby obtaining a minimum energy consumption which also suits for low operating frequencies. In order to attain more extensive application, scaling supply voltage to medium-voltage region is an attractive approach especially suiting for mid performances. Technology scaling also demands a decrease in both supply voltage (V_{DD}) and threshold voltage (V_{TH}). However concept of sub-threshold region works with only low frequency application. Hence Single Phase Adiabatic Dynamic Logic is developed to work with high frequency applications. Another low power technique namely GATE DIFFUSSION INPUT (GDI) is implemented in the project for sequential circuits. The circuit design and simulation results are simulated in 0.18µm TSMC technology with the supply voltage of 0.3 to 0.4V and delay of 60ns using CADENCE VIRTUOSO spectre simulator.

Index Terms:–Power consumption, Gate Diffusion Input, Adiabatic Dynamic logic.

I. INTRODUCTION

To improve the performance of logic circuits, the traditional way is the CMOS technology; we know that the CMOS technology suffers from many advantages considering one among them is power. In today, many of the applications are dealing with low power, Compaq and the speed. So considering above parameters, have introducing a new low power GDI technique which resulted in the development of many logic circuits with limited transistors. However, technology scaling has made power density a major factor in digital systems. Many design architectures and techniques have been developed to reduce power dissipation, and low-power has become one of the primary focuses of digital design.

This paper describe power consumption, area and speed of the sequential circuits, working under subthreshold region using two low power techniques ADIABATIC logic and GDI technique.

II. POWER CONSUMPTION COMPONENTS

High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heat sink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency [17, 19].
Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

2.1.1 Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter.If the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). [1-6] the output voltage is VCC, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from

VCC to GND, the resultant quiescent (steady-state) current is zero; hence, static power consumption (Pq) is zero.

The source drain diffusion and N-well diffusion form parasitic diodes. The parasitic diodes are between the N-well and substrate. These parasitic diodes are reverse biased; only their leakage currents contribute to static power consumption. The leakage current (I_{lkg})of the diode is described by the following equation:

$$I_{lkg} = i_s \left(e^{\frac{qv}{kT}-1}\right) \quad (1)$$

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation (2).

$$P_s = I_c * V_s \quad (2)$$

The leakage current I_{CC} (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or PS, and can be calculated by equation 3.

$$P_s = V_{cc} * I_{cc} \quad (3)$$

Another source of static current is ΔI_{CC}. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

2.1.2 Dynamic Power Consumption

The dynamic power consumption of a CMOS IC [7] is calculated by adding the transient power consumption (P_T), and capacitive-load power consumption (P_L).

(A) Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from V_{CC} to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, has a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance. Transient power consumption can be calculated using equation (4).

$$P_T = C_{pd} * V_{cc}^2 * f_i * N_{SW} \quad (4)$$

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{pd} can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). C_{pd} is discussed in greater detail in the next section.

(B) Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency

$$P_L = C_L * V_{CC}^2 * f_a * N_{SW} \quad (C_L \text{ is the load per output}) \quad (5)$$

In the case of different loads and different output frequencies at all outputs, equation (6) is used to calculate capacitive-load power consumption.

$$P_L = \sum (C_{Ln} * f_{on}) * V_{CC}^2 \quad (6)$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions and can be expressed as shown in Equation (7), equation (8) (single-bit switching), and equation (9) (multiple-bit switching with variable load and variable output frequencies).

$P_D=P_T+P_L$ (7)

$P_D=(C_{pd} * f_I * V_{cc}^2)+(C_L * f_o * V_{cc}^2)$ (8)

$P_D=[(C_{pd} * f_i * N_{sw})+\sum(C_{LN} * f_{on} *)]*V_{cc}^2$ (9)

$P_{total} =P_{static} +P_{dynamic}$ (10)

2.2 POWER AND ENERGY

It is important at this point, to distinguish between energy and power. The power consumed by a device is, by definition, the energy consumed per unit time. In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T_{op}), hence,

$E=\int_0^{Top} p(t)dt$ (11)

Here, the power of digital CMOS circuit is given by

$P=CV_{DD}V_Sf$ (12)

$E = nV_{DD}V_{SS}$ (13)

It is important to note that the energy per operation is independent of the clock frequency. Reducing the frequency will lower the power consumption but will not change the energy required to perform a given operation [29]. Since the energy consumption is what determines the battery life, it is imperative to reduce the energy rather than just the power. It is, however important to note that the power is critical for heat dissipation considerations.

2.3 PROPAGATION DELAY

Several observations can be made from the analysis: PMOS was widened to match resistance of NMOS by 3 - 3.5. This was done to provide symmetrical H-to-L and L-to-H propagation delays. This also triples the PMOS gate and diffusion capacitances. It is possible to speed-up the inverter by reducing the width of the PMOS device (at the expense of symmetry and noise margins)! Widening PMOS reduces tpLH by increasing the charging current, but it also degrades the tpHL by causing a larger parasitic capacitance. This implies that there is an optimal ratio that balances the two contradictory effects.

Consider two identically sized CMOS inverters. The load cap of the first gate is approximated by:

$C_L=(C_dp1 + C_dn1)+(C_gP2 + C_gn)+C_W$

(14)

Now assume PMOS devices are made b times larger than NMOS

$C_dp1=\beta C_dn1 \& C_gp1 = \beta C_gn$ (15)

$C_L = (1 + \beta)(C_dn1 + C_gn2) + C_W$ from equation 14

$t_p=t_pHL + \frac{t_pLH}{2} = .69C_l(R_{eqn} + R_{eqp}/\beta)$ (16)

$t_p=.345(1+\beta)C_dn1 + c_gn2)+C_W)R_{eq}n(1 + \gamma/\beta)$ (17)

Propagation delay for the inverters is easier to calculate and is data independent. This delay has been calculated as [28]

$t_{pd\ inv} = KC_{load}V_{DD}/I_o \exp[\frac{V_{DD}-V_{th}}{\frac{nKt}{q}}]$ (18)

When focusing on the pure design, performance is most often expressed by the duration of the clock period (*clock cycle time)*, or its rate (*clock frequency*). The minimum value of the clock period for a given technology and design is set by a number of factors such as the time it takes for the signals to propagate through the logic, the time it takes to get the data in and out of the registers, and the uncertainty of the clock arrival

times. At the core of the whole performance analysis, however, lays the performance of an individual gate. The *propagation delay tp* of a gate defines how quickly it responds to a change at its input(s). It expresses *the delay experienced by a signal when passing through a gate*. Because a gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The *tpLH* defines the response time of the gate for a *low to high* (or positive) output transition, while *tpHL* refers to a *high to low* (or negative) transition. The propagation delay *tp* is defined as the average of the two.

$$t_p = t_pLH + \frac{t_pHL}{2} \qquad (19)$$

III. SPADL

Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability. The main idea behind adiabatic design is to transfer charge between circuit capacitances and a time varying power-clock source. This technique enables the charge transfer to occur in a controlled manner, limiting the current and thus decreases the energy dissipation across the active devices. Adiabatic circuitry can potentially achieve sub-CV2 energy dissipation per cycle. Previously reported adiabatic logic styles need multi-phase clocking which make them sensitive to clock skew and may severely limit to their high-frequency performance. In order to make adiabatic logic circuits more feasible and practical in VLSI CMOS applications, single-phase operation of the circuits would be needed.

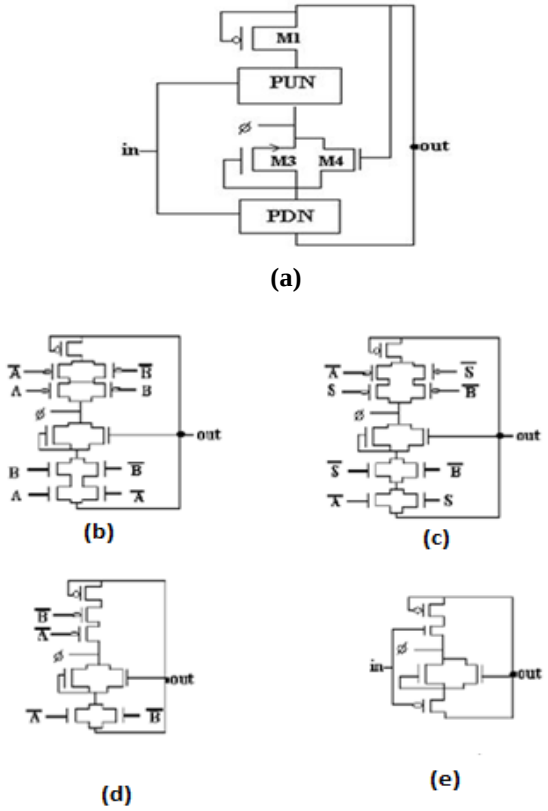


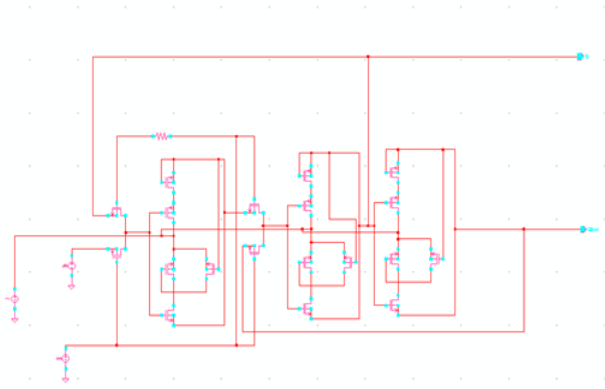
Fig 1 SPADL (a) INVERTER, (b) XOR, (c) 2*1MUX, (d) AND, (e) BUFFER

2) a Configuration and Operation

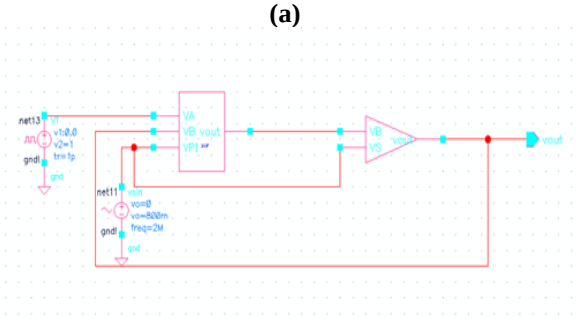
Fig 1(a) shows the general configuration of SPADL logic block and SPADL inverter. on basis of applied logic inputs, either pull up or pull down network (PUN or PDN) will be ON at any time instant, the charging and discharging operations of output (out) node is described as follows: [9]

- When PUN is ON and ‘out’ is low, if supply clock (φ) ramps up ‘out’ node will be charged through PUN→M1 by following φ closely and higher logic will be obtained at out node. When φ ramps down, charges will be stored at ‘out’ node, as they cannot flow back to the supply clock (φ) due to reverse biased M1.
- When PDN is ON and ‘out’ is high, if φ ramps down, charge stored at ‘out’ node flows back to the supply clock (φ) through the PDN→M3and M4.
- When PUN is ON and ‘out’ is high, if φ ramps up ‘out’ node will not transit for that clock period. So voltage level of ‘out’ node will not vary.

- When PDN is ON and 'out' is low, 'out' node voltage will not transit for that complete clock cycle, Though due to presence of diodes in charging and discharging paths degraded output swing will be obtained yet the lower swing will be improved significantly as the lower resistive parallel paths are provided from output to the supply clock by the SPADL logic.



(a)



(b)

Fig 2 SPADL (a) D FLIPFLOP, (b) T FLIPFLOP

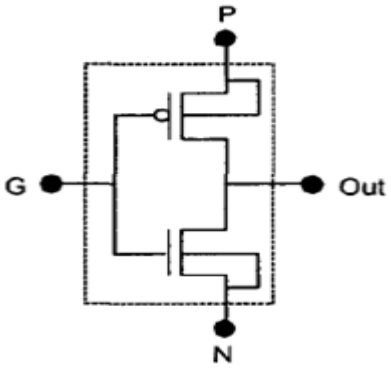
As sub-threshold conduction takes slow flow of electronics and works in low frequencies. But SPADL works with high frequency. Because of this limitation we introduce another new low power GDI technique. This technique is efficiently working in sub-threshold region by occupying low area this can be said by, for example a normal CMOS AND gate requires 6 transistors, by using GDI technique it requires 2 transistors by observing this the number of transistor count has been decreased hence the further description of this . As our aim is to design sequential circuits, firstly we designed basic logic gates using GDI technique and then have implemented D and T flip-flop with operating frequency of 100k to 500k Hz's and with the voltage of 300mV to 400mV. Therefore, it is shown through the simulation that these circuits consume low power with low energy efficiency and appropriate delays

IV. GDI

These techniques are taken in to consideration to show that the sequential circuits are good enough to work with low power. Several methods for reducing the power consumption of flip-flops have been proposed. Among the most promising method is to reducing the power supply voltage offers the most direct and dramatic means of reducing the power consumption is the CMOS GDI. GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low power circuits, using reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving power characteristics and allowing simple Shannon's theorem-based design by using small cell library. Using CMOS GDI under sub-threshold operation is considered to be the most energy-efficient solution for low-power applications where performance is of secondary importance

GDI method is based on the use of a simple cell as shown in Figure3 At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences:

Fig 3 GDI INVERTER



- GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
- Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table 1. Various Logic Functions of GDI Cell for different Input Configurations

A	B	Functionality	F1
0	0	*pMOSTrans Gate*	V_{Tp}
0	V_{DD}	*CMOSInverter*	V_{DD}
V_{DD}	0	*nMOS Trans Gate*	0
V_{DD}	V_{DD}	*CMOSInverter*	0

Table 2. Input Logic States vs. Functionality and Output Swing of F1 function

A. Operational analysis of GDI cell

From above table 2, In order to understand the effects of low swing problem in GDI cell, we suggest the following analysis, based on the example of **F1** function, and can be easily extended to use in other GDI functions. Table1 presents a full set of logic states and related functionality modes of F**1.** [23-26].

As can be seen from Table 2, the only state where low swing occurs in the output value is A=O, B=O. In this case the voltage level of **F1** is V_{tp} (instead of expected OV) because of poor high to- low transition characteristics of PMOS pass-transistor**.** It is obvious that the only case (among all the possible transition's) where the effect occurs is the transition from the **A=O,** B=V_{DD} to A=O, B=O.

The fact that demands a special emphasis is that in about **50%;** of the cases (for B=l) the GDI cell operates as a regular CMOS inverter, which is widely used as a digital buffer for logic level restoration. In some

of these cases, when V_{DD}=' 1 ' without a swing drop from the previous stages, a GDI cell functions as an inverter buffer and recovers the voltage swing.

4.1. GDI Sequential circuits

Sequential circuits are memory based devices which is also called as "feedback". The stable output of a combinational circuit does not depend on the order in which its inputs are changed. The stable output of a sequential circuit usually does depend on the order in which the inputs are changed. We usually focus on clocked sequential circuits, in which the circuit changes state at fixed times in a clock cycle. Clocked circuits are easier to design and understand.

All sequential circuits depend on a phenomenon called gate delay. This reflects the fact that the output of any logic gate (implementing a Boolean function) does not change immediately *when* the input changes, but only some time later. The gate delay for modern circuits is typically a few nanoseconds.

A. GDI D Flip-flop

The cross-coupled inverters ensure that strong signals are passed from the multiplexers and block any reverse currents through the multiplexers. This flip-flop comprises 12 transistors, a relatively small number, substantially reducing area and capacitance.

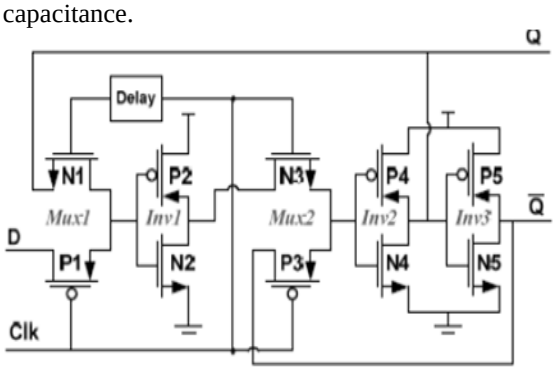


Fig 4 Modified GDI D flip-flop

A modification can be implemented to this basic architecture to improve the setup time and reduce area. The architecture is as given in [28] this can be achieved by removing the first stage feedback inverter and passing it to second stage. This design comprises of 10 transistors plus a delay element that can be implemented with a resistor or a transistor. This architecture takes the advantage of the feedback in second stage making first stage redundant. This way the transistor count is reduced achieving smaller area and the setup time can be reduced by the addition of inverter. Here the delay should be considered and estimation of the delay is obtain from [26]

B. GDI T flip-flop

A novel implementation of a GDI TFF is shown in Fig. 3.4. It is based on the Master-Slave connection of two GDI Latches and some gates. Each latch consists of four basic GDI cells, resulting in a simple eight-transistor structure and gates consists six transistors in order that related with latch. The components of the latch circuit can be divided into two main categories; GDI gate and inverter. GDI gate uses two transistors and controlled by the Clock signal. Clock signals fed to the gate of transistors and create two alternative states: one state is when the Clock is low and the signals are propagating through PMOS transistors and create transient state and other one is when the Clock is high and the prior values are maintained due to conduction of the outputs. In this state, GDI gates holding state of the latch.

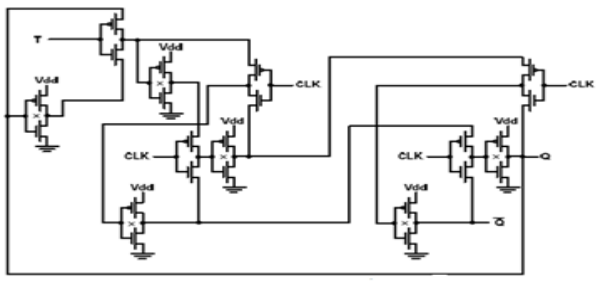


Fig 5. GDI T Flip-flop

Other gates for main T flip flop are inverter gates. They are responsible for maintaining the complementary values of the internal signals and the circuit outputs. Note that the size of the p-channel transistor is wider than that of the n-channel transistor. This width difference is not needed for functionally correct operation. Rather, it somewhat compensates for the difference in the motilities of n-channel and p-channel transistors. The effective mobility of n-channel transistors is between two and four times that of p-channel transistors. These inverters has important role for swing restoration and improved driving abilities of the outputs, it's buffering of the internal signals and create suitable output current for driving of load. [26] The same delay is estimated for all the inverters given as propagation time delay for inverter but other GDI gates are also calculated taking rise time, fall time, load capacitance, set up & hold time of the generated clock to the data input.

V. MOSFETS IN THE SUB-THRESHOLD REGION

As mentioned earlier that making GDI technique to work under sub-threshold, so here describing briefly the working of MOSFET in sub-threshold region and showing what are the parameters effecting MOSFET in this region. Several papers have focused on evaluating the effectiveness of different circuit styles in the sub-threshold regime. The Vdd–Vt space was comprehensively mapped through simulations to obtain the optimal point for operation for traditional CMOS for a variety of performance levels [31].

Sub-threshold Current--- "Off" is not totally "Off" MOSFET transistor conducts in three regions, here focusing on sub-threshold region, this shows that current of an MOSFET transistor occurs when the gate-to-source voltage (VGS) of a transistor is lower than its threshold voltage (VTH). When VGS is larger than VTH, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as strong-inversion, as more minority carriers are present in the channel than majority carriers. When VGS is lower than VTH, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak-inversion. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (VDD) is lowered below VTH, the circuit can be operated using the sub-threshold current with ultra-low power consumption. [21] Weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of VTH, sub-threshold circuits are very sensitive to process variations and temperature fluctuation.

Circuit speed improves with increasing Ion, therefore it would be desirable to use a small Vt. Can we set Vt at an arbitrarily small value, say 10mV? The answer is no. At Vgs<Vt, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at Vgs<Vt is called the sub-threshold current. This is the main contributor to the MOSFET off-state current, Ioff. Ioff is the Id measured at Vgs=0 and Vds=Vdd. It is important to keep Ioff very small in order to minimize the static power that a circuit consumes even when it is in the standby mode.

$d\varphi_s/dV_{gs} = C_{ox}/(C_{ox}+C_{dep}) = 1/\eta$ (20)

$\eta = 1+C_{dep}/C_{ox}$ (21)

Integrating Eq. (14) yields

$\varphi_s = \text{constant}+V_g/\eta$ (22)

Ids is proportional to n_s, therefore

$$I_{ds} \propto n_s \propto e^{q\varphi_s/kT} \propto e^{q(\text{constant}+V_g/\eta)/kT} \propto e^{qV_g/\eta kT} \quad (23)$$

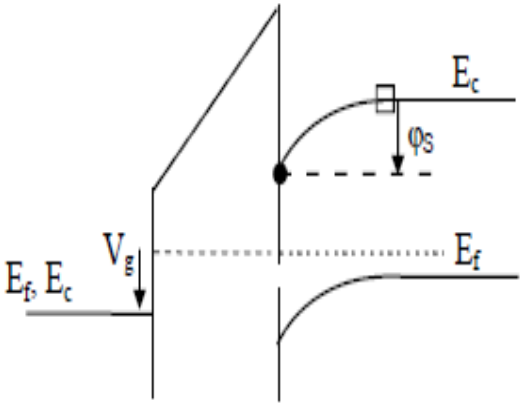
The practical definition of Vt in experimental studies is the Vgs at which Ids=100nA ×W/L.(Some companies may use 200nA instead of 100nA.)1. Eq. (16) may be rewritten as.

$I_{ds}(nA) = 100W/Le^{(q(Vgs-Vt)/nKT}$ (24)

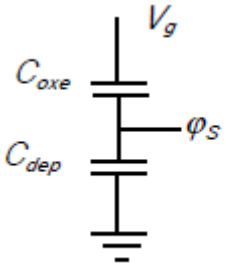
$S = n60mV(T/300)$ (25)

$I_{ds}(nA) = 100\ W/L\ e^{q(Vgs-Vth)/nKT} = 100\ W/L\ 10^{(Vgs-Vth)/S}$ (26)

$I_{off}(nA) = 100\ W/L\ e^{-qVt/nKT} = 100\ W/L\ 10^{-Vt/S}$ (27)



(a)



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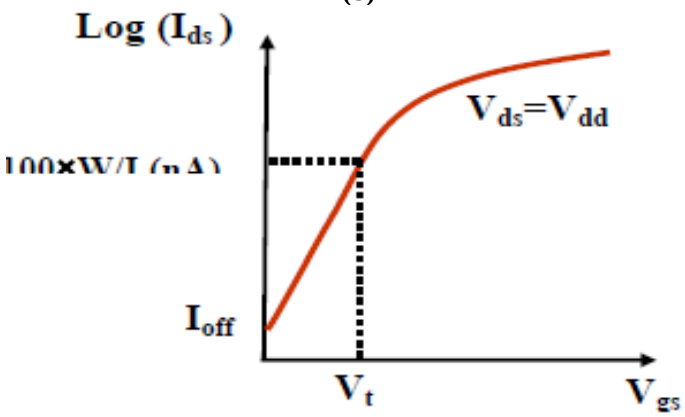

(c)

Fig 6 (a) When Vg is increased, Ec at the surface is pulled closer to Ef, causing ns and Ids to rise; (b) equivalent capacitance network; (c) Subthreshold IV with Vt and Ioff.

For given W and L, there are two ways to minimize Ioff illustrated in Fig.6. (c). the first is to choose a large Vt. This is not desirable because a large Vt reduces Ion and therefore increases the gate delays. The preferable way is to reduce the subthreshold swing. S can be reduced by reducing □ □ □ □ That can be done by increasing Coxe (see Eq.21), i.e. using thinner Tox, and by decreasing Cdep, i.e.increasing Wdep.**2** an additional way to reduce S, and therefore to reduce Ioff, is to operate the transistors at a lower temperature. This last approach is valid in principal but rarely used because cooling adds considerable cost.

$$I_{subt\,hr} = I_o * e^{[V_{gs}-V_{th}/nV_T]} * \left(1 - e^{\frac{-V_{Ds}}{V_t}}\right) * e^{I]V_{Ds}/nV_t} \qquad (28)$$

$$I_{subt\,hr} = \mu_o C_{ox} W/L(n\text{-}1)V_t^2 \qquad (29)$$

5.1. I_{LEAK} Components of MOSFET devices

Different physical phenomena contribute to the leakage current causing the static consumption when one or more transistors are in VDD to GND paths are in off state. These currents are listed next, and are

separated in to five classes according to the physical origin of the current [30].Tunnelling current of electrons across thin gate oxide between the gate and the substrate IC due to high electric field in the gate oxide. The responsible mechanism in nano-metric devices is direct tunnelling through the oxide bands.

Sub-threshold conduction producing leakage currents ISUBTH, which flow from drain to source. When MOSFET has a gate voltage below the threshold voltage, the device is in weak inversion or depletion. When gate to source voltage VGS is applied, even before the device threshold voltage, sufficient charge carriers are on the surface region that can still create a significant current flow.

Gate induced drain leakage IGIDL currents flowing from drain to substrate. The currents are due to tunneling of electrons from the valence to conduction band in the transition zone of the drain substrate junction below the gate to drain overlap region where a high electric field exists.

Reverse biased pn junction in the circuit. The leakage current ID of reverse biased pn junction are due to various mechanisms such as diffusion thermal generation in depletion region of the junctions. In nano-metric technologies, junction tunneling current due to bulk band to band tunneling current IBTBT may appear.

To limit the energy and power increase in future CMOS technology generations, the supply voltage (Vdd) will have to continually scale. The amount of energy reduction depends on the magnitude of Vdd scaling. Along with vdd scaling, the threshold voltage (V,) of MOS devices will have to scale to sustain the traditional 30% gate delay reduction. These vdd and V, scaling requirements pose several technology and circuit design challenges. One such challenge is the rapid increase in sub-threshold leakage power due to VI scaling. Should the present scaling trend continue it is expected that the sub-threshold leakage power will become a considerable constituent of the total dissipated power. In such a system it becomes crucial to identify techniques to reduce this leakage power component. It has been shown previously that the stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. In rest of the paper the term leakage refers to sub-threshold leakage.

5.2 Sub-threshold Leakage

Since the early days of the MOS transistor, its switching capability has been exploited by a wide variety of applications. By applying a high or low voltage on the gate contact, the current flow between source and drain can be switched on or off, respectively. The off-state current was supposed to be very small; in fact, early analytical models for the electrical behaviour of MOS transistors like the low-level SPICE models were even assuming a zero off-state current. Commonly used equations for deriving the drain current were based on the well-known quadratic transfer curve of a MOS transistor. Below a certain gate-source voltage, called ``threshold voltage", the drain current was supposed to be zero [30, 31].

As a result, the off-state current gradually became a limiting factor for down-scaling the

Under weak inversion the channel surface potential is almost constant across the channel and the current flow is determined by diffusion of minority carriers due to a lateral concentration gradient. Under strong inversion there exists a thin layer of minority carriers at the channel surface and a lateral electric field which causes a drift current. The moderate inversion regime is considered a transition region between weak and strong inversion where both current flow mechanisms coincidently exist. In the weak-inversion (or sub-threshold) regime, the drain current depends exponentially on the gate-source voltage

$$I_{d,weak} \propto \exp\left(\frac{V_{gs}}{nV_t}\right) \qquad (30)$$

The exponential sub-threshold behavior can be explained by the exponential dependence of the minority carrier density on the surface potential which, itself, is proportional to the gate voltage. On a semi-logarithmic scale the transfer (Id-Vg) curve in the sub-threshold regime will, therefore, be a straight line, the slope of this line is called ``sub-threshold slope". The inverse of this slope is usually referred to

$$S = nV_T \ln(10) \qquad (31)$$

Due to the bulk effect the sub-threshold swing of a conventional MOS transistor in bulk technology will always be higher than a certain optimum value which is roughly 60 mV/dec at room temperature, and which can be calculated by setting equal to 1 which means that the bulk effect is fully suppressed. In a realistic case will always be larger than 1. Therefore, the actual sub-threshold swing will always be larger than Sopt depending on how well the channel surface potential can be controlled by the gate contact.

A small sub-threshold swing is highly desired since it improves the ratio between the on- and off-currents. This requires that the bulk charge in the depletion region under the channel changes as little as possible when the gate voltage varies therefore C_b should be small.

The above description shows the working of NMOS in subthreshold region. If it PMOS is just opposite to NMOS ie if NMOS working in suubthreshold region then PMOS is said to work in saturation, if Vgs < Vth PMOS starts conducting from linear to saturation and it only conducts when input is "0". The effects that occur in NMOS under subthreshold region will also occur in PMOS. Not only above mentioned parameters are

effected the other parameters are also considered like hot- carrier effect, DIBL, punch through, gate leakage etc can refer to [23-27]. To calculate leakage currents $I_{leakage}$ components are considered.

VI. CONCLUSION

The primary goal of this paper work is not only to provide an efficient result in low power VLSI design but also shows a successful try in terms of reduction of power dissipation. The basic low power CMOS cell structure are designed using CMOS logic style and another effective approach Gate Diffusion Input technique. The entire CMOS cell structures implemented in the project are designed in cadence IC Design Architect using standard TSMC 0.18 µm Technology. As the main concern is power dissipation so after the schematic design and the simulation, different values of power dissipation at different values frequencies has been taken for both logic style. The circuits are operated under sub-threshold region with supply voltage of 300mV to 400mV and the operating frequency ranges from 100-500k Hz's and with different load capacitance. With gate diffusion input technique, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of GDI technique, the power saving of up to 40 to 60 %can be reached and occupy less area.

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